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A multilevel memristor–CMOS memory cell as a ReRAM

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ABSTRACT

Memristor is a newly invented device and since it has been found, has drawn a lot of attention from integrated electronics designers because of its nanometer size and special electrical properties. One of the most significant characteristics of a memristor is its memory property. In this paper, a nonvolatile memory cell, based on the hybrid structure of memristor and Complementary Metal-Oxide-Semiconductor (CMOS) is proposed which can be used as a resistive Random Access Memory (RAM). This cell can store data in either binary or non-binary (multilevel) logic, increasing the amount of storable data per square area of a memory chip by increasing the levels of stored data. The methodologies of work with this multilevel logic and data saving and retention are discussed and the suitable one is chosen. The proposed memory cell has a read time comparable to other RAMs and flash memories and percent's of area reduction per two bits of data with at least 50% increase in reading speed – for ternary logic – per data. Power consumption is also reduced. The buffer for this cell corresponding to ternary logic is also presented.

1. Introduction

Memristor as a new electrical component was first predicted by Chua in 1971. This prediction was based on the symmetry between mathematical definitions of basic electrical components, i.e. resistor, capacitor and inductor [1]. But this newly introduced element was given a lot of attention when HP published its finding about memristor in the Nature journal in 2008 [2]. One very important reason why memristor was not found earlier is that the notable changes in the device resistance after applying a constant stimulus to it as the memristance property of a device is dominant only in nanometer scale. As a result the physical implementation of the first memristor was delayed until 2008.

Memristor has vast applications, which analog to digital converters and memory elements in logic circuits are two examples of them [3–7]. Neural and neuro-fuzzy networks [5,8,9], programmable logic and processing configurations [4], chaotic circuits [7], and most importantly memory devices, are basic applications predicted for memristor as an electronic element. The interesting fact about memory property in memristor is that not only one single memristor can be fabricated on a dense surface but also it can be programmed on values which are going to be saved in simple structural designs.

Memristor has very special characteristic that makes it desirable to be used in VLSI circuits. It has a switching property that can be controlled by its current or voltage. This means that the switching function can be realized by a memristor as a two-terminal component versus transistors with three terminals. The switch works by changing the resistance (memristance) of the device between a low and a high value. These values depend on memristor parameters and fabrication process. The ratio of the high to low resistances in the memristors fabricated until now is more than 1000 [4] indicating a very good switching behavior. Another important characteristic of this device is its small size, in the order of nanometer, that is ideal for today high density integrated circuits. Memristor fabricated in the paper by Strukov et al. [2] has about than 10 nm width that is smaller than the today's MOSFETs channel length of a standard CMOS technology with 22 nm channel length. It is also possible to fabricate memristors with even smaller size. Memristor is compatible with CMOS fabrication process and 3-D stack up, leading to very high density and overcoming 2-D structure limitations as stated in the paper by Xia et al. [4]. It can be predicted that hybrid memristor–CMOS circuits will have very high functionality in electronic circuits in near future.

The most important specialty of memristor is its ability to memorize its previous state; meaning, it can act as a memory cell. This memory is not similar to electric or magnetic energy which is stored on a capacitor or in an inductor. In fact, it is not similar to

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stored state in a common RAM memory either. The memorizing of the previous state is related to the memristance property of the device. This property can get any value between its high and low resistances. Moreover, a memory made from memristor is non-volatile. Therefore, in the absence of any stimuli, it keeps its resistance unchanged for more than 10 years [10]. This property can be adopted to design a memory cell using a single memristor as the key element for data storage.

Almost all memory storage devices available today store data in binary logic, that is, any data on a memory cell has a value of "0" or "1." In these designs power consumption and amount of data per number of transistors are important parameters and should be taken into account.

In this paper, we propose a memory cell based on hybrid memristor–CMOS structure that is able to store data in binary, ternary, quaternary, etc. without the need for much overhead circuitry. This multilevel structure increases the amount of data stored on each cell, resulting in more data density on the whole storage device. The difference between any levels of logical data to be stored is mainly based on the buffer structure which is placed after the cell whereas the core cell topology is mostly the same. In this paper, the problems of acceptable data margins and restrictions on increasing the number of logical levels, along with a comparison between similar binary and multilevel storages are discussed. Here, for simplicity after introducing main cell, we focus more on a ternary logic and simulation results are presented based on this type. Even though, as mentioned earlier, the topology can be used in logics with more levels.

It is predicted that using memristors in hybrid, multilevel structures makes it possible to design devices that use multilevel memory and logic in their main processing units. This leads to faster computations with more straight-forward design [11].

This paper is organized as follows: Section 2 introduces the memristor and its models with emphasis on multilevel memory states. In Section 3, the proposed memory cell topology is introduced and its functionality is described. The buffer structure and other design considerations and restrictions are also introduced in this section. In Section 4, simulation results and comparison to some similar circuits are provided and finally Section 5 gives a conclusion on the paper.

2. Multilevel memristor memory

The basic physical definition of a memristor is stated as

$$d\varphi = M \cdot dq \tag{1}$$

where $d\varphi$ and dq are infinitesimal values of magnetic flux and electric charge, respectively and M is the memristance of the device that is a function of electric charge [1]. The memristor device which was introduced by HP in the paper by Strukov et al. [2] can be modeled by two resistors in series, as shown in Fig. 1(a), with the I–V relationships as

$$v(t) = M(q(t)) \cdot i(t) \tag{2}$$

$$M(q(t)) = R_{on} \cdot \left(\frac{w}{D}\right) + R_{off} \cdot \left(1 - \frac{w}{D}\right). \tag{3}$$

In the above equations R_{on} is the lowest possible resistance of the memristor and R_{off} is the highest one, D is the length of the device and w is an imaginary boundary between the two resistances, which in general is known as "state" of the device. Equation that determines changes in w is written as is mentioned in the paper by Strukov et al. [2]

$$\frac{dw(t)}{dt} = \frac{\mu_v \cdot R_{on}}{D} \cdot q(t) \cdot F(w, D) \tag{4}$$

where μ_v is the average dopant mobility in memristor and $F(w, D)$ is a window function. The window function causes the right side part of Eq. (4) to drop when w reaches each boundary ensuring not to exceed the limits of "0" and "D". Some of the nonlinear electrical characteristics of the memristor devices and the ability to better fit the device models can also be addressed through the window function [12]. Several window functions have been proposed by Biolek et al. [13], Joglekar et al. [14], Prodromakis et al. [15] and Kvatinsky et al. [12]. Table 1 compares some of the important characteristics of these functions by introducing their mathematical relationship.

The window function introduced by Biolek et al. [13] is used in this paper, since it is symmetric, handles the boundary conditions well and can be fit well to memristive models. The nonlinear behavior of the device at boundaries [2] is also possible to be well modeled using Biolek's window function. The relationship for this window is given by Eq. (5). Parameter "p" is an even number and controls the nonlinearity of the rate of changes in w at the boundaries

$$F(w, D) = \left(1 - \left(\frac{w}{D} - sgn(-i)\right)^{2p}\right) + \delta \tag{5}$$

where $sgn(i)$ is the sign function of the current flowing through the device. If $i \geq 0$ wehave $sgn(i) = 1$, and for $i < 0$, $sgn(i) = 0$. To avoid the stuck problem when w reaches any of the boundaries, parameter $0 < \delta < 1$ is also added. Fig. 2 shows the plot of the window function $F(w, D)$ versus w/D in which the variable p has been used as a parameter.

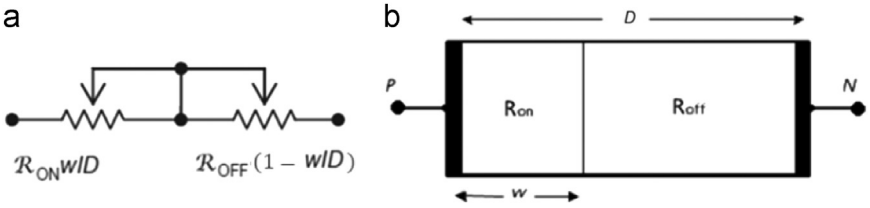

Fig. 1. A memristor device model: (a) two resistors in series, (b) physical model [2].

Table 1
Comparison of window functions [12].

Window function	Biolek	Joglekar	Prodromakis	TEAM
Mathematical equation	$f(w)=1-(w/D-stp(-i))^{2p}$	$f(w)=1-(2w/D-1)^{2p}$	$f(w)=j(1[(w-0.5)^2+0.75]^{2p})$	$f_{on,off}=exp[exp(\|x-x_{on,off}\|/w_c)]^*$
Symmetry	Yes	Yes	Yes	Not necessarily
Boundary conditions problem	Yes	No	Partially yes	Partially yes

* In TEAM model, window function is defined mainly by fitting the relationships to a Simmons tunnel barrier model.