Microelectronics Journal 46 (2015) 1343–1350

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A sub-mW pulse-based 5-bit flash ADC with a time-domain fully-digital reference ladder

Nikola Katic*, Radisav Cojbasic, Alexandre Schmid, Yusuf Leblebici

Swiss Federal Institute of Technology (EPFL), Batiment ELD, Station 11, 1015 Lausanne, Switzerland

ARTICLE INFO

Article history:
Received 8 February 2015
Received in revised form
26 July 2015
Accepted 28 September 2015
Available online 6 November 2015

Keywords:
Flash ADC
Time-to-digital converter
Fully-digital
Pulse-based
Time-domain

ABSTRACT

The concept of time-domain reference-ladder for the implementation of fully-digital flash-ADCs is proposed in this work. The complete reference ladder is implemented using only digital circuits. Based on this concept, a flash ADC is proposed and implemented in this work using digital circuits, one comparator and a customized sample-and-ramp circuit. An unconventional time-to-digital conversion (TDC) technique is introduced which performs the complete conversion within a single clock cycle. The measurement results show that the proposed 5-bit converter achieves an 80 MHz sampling rate while consuming 900 μW of power from the 1.8 V supply voltage. The prototype ADC is developed in a 180 nm standard CMOS technology and achieves the power efficiency of 445 fJ/conversion which is comparable to many existing state-of-the-art flash ADCs. The measured performance is achieved without any design optimization or circuit calibration techniques confirming the promising benefits of the proposed topology. Thanks to the fully-digital structure, the circuit enables a robust and compact implementation which is very convenient for interleaving and beneficial for many potential applications.

1. Introduction

Digital circuits are significantly less sensitive to noise, device mismatch and integrated circuit parasitic effects than their analog counterparts. Moreover, conventional analog design techniques require signal linearity which is especially important in analog-to-digital converter (ADC) design. However, linearity has been increasingly hard to achieve in modern sub-micron CMOS processes due to low supply voltage and reduced intrinsic gain of the MOSFET devices. Digital CMOS circuits operate rail-to-rail; they are essentially non-linear, hence they do not rely on signal linearity. Accordingly, recent trend in ADC design increasingly promotes digital implementations of the converter core [1,2]. In addition, digital circuits can perform error-correction tasks very efficiently which has motivated the studies of digitally-assisted analog circuits for over a decade [3]. Nowadays, digital calibration is a necessity for efficient high and medium resolution ADCs [4–6] and is starting to emerge even in low resolution ADCs [7].

Time-to-digital conversion (TDC) represents an additional recent research focus in the field of ADC design. Thanks to the CMOS technology scaling, the CMOS gate delay has reached the pico-second range which allows a very high time-domain (ps) resolution [8–12]. TDCs process signals in time-domain and can be based on mainly digital circuits, consequently exploiting all the benefits of digital operation. Conveniently, TDCs utilize the high speed of modern CMOS technologies (high cutoff frequency f_T) and do not rely on voltage amplitudes, which allows them to operate at a low supply voltage. Nevertheless, achieving the high resolution in time-domain is not as straight-forward as it might seem. Conventional flip-flops (latches) which are needed to sample the high-speed data, suffer from relatively high setup and hold-times. Moreover, latch regeneration process can be very sensitive to input signal amplitudes and device mismatch. If not taken into consideration, these circuit non-idealities can set the limit to the achievable time resolution, therefore limiting the overall performance of the converter. Design in [8] uses time multipliers to multiply the timing residue created by the long latch regeneration process. This approach effectively eliminates the problem of long latch regeneration and creates fine-coarse converter topology (similar to folding) ADC. A similar approach is used in [9] where a different algorithm (called Redundant Remainder Number System) is used to handle the timing residues and create a folding-flash TDC architecture. In order to ensure narrow sampling window, design in [10] implements a sense-amplifier based latches. Designs presented in [11] and [12] use dynamic latches that are typically less sensitive to timing issues and uncertainties, but often consume more power than static latches. Dynamic latches with pulse-triggered sampling are used in this work because they are very

* Corresponding author.
E-mail address: katic.nik@gmail.com (N. Katic).

http://dx.doi.org/10.1016/j.mejo.2015.09.017
0026-2692/

robust when it comes to timing uncertainties and have very low setup and hold times. Another important difficulty of Time-to-Digital conversion is an effective conversion of the input voltage to time domain. An effective solution is used in [12], where the input voltage is sampled and compared to the dual ramp reference, generating pulse-width-modulated (PWM) digital output. Similar concept with a different implementation (sample-and-ramp) is used in this work in order to deal with the input voltage-to-time conversion.

Despite the previously mentioned trends, most state-of-the-art flash ADCs use some form of resistive reference ladder and focus on improvements and optimizations of the existing concepts [13–35]. An interesting design is presented in [13] which uses TDC technique to directly implement a flash converter, however the design still uses a resistive reference ladder at the input stage. The main contribution of this paper consists of replacing the existing concept of the flash ADC's resistive reference ladder with the time-domain reference ladder which offers a straight-forward and efficient digital implementation. This approach results in a digital flash ADC topology with only one comparator. The comparator's pre-amplifier and the sample-and-ramp circuit are the only design blocks operating in the analog-domain. Following the proposed approach, flash ADCs can become fully digital circuits and benefit from digital and time-domain operation. Such implementations are more convenient for low supply voltage operation and for the implementation in the existing advanced nano-meter CMOS technologies. This paper discusses the concept of time-domain reference ladder, the fully-digital flash ADC, and presents a prototype flash ADC design implemented in a 180 nm CMOS technology. The paper is organized as follows. The digital reference ladder concept is explained in Section 2. Section 3 discusses the top-level architecture and the main features of the proposed flash ADC. A specific output decoding scheme implemented to increase the number of available quantization levels and the reliability of the conversion is explained in Section 4. The input-voltage to time-domain converter (voltage-to-time converter, VTC) is discussed in Section 5. The measurement results are presented in Section 6 and the paper conclusion is provided in Section 7.

2. Time-domain pulse-based digital reference ladder

The core function of a conventional flash ADC can be broken down into two fundamental steps, (1) the generation of reference (quantization) voltage levels, and (2) the comparison of the input analog voltage with the generated references. In a conventional flash-topology, the first step is performed by a resistive ladder while the comparison with the generated references is performed by a set of comparators (one per reference). This concept is illustrated in Fig. 1(a). Nevertheless, the same functionality can be achieved by the digital circuit in Fig. 1(b).

A reference clock signal (CLK_{REF}) is generated as a delayed version of the input sampling clock (CLK_{SMPL}) to allow for the input sampling before the reference ladder starts its operation (this will be explained in more detail in Section 5). The reference clock is used as an input to an array of 32 inverters which creates a family of 16 clock signals delayed with respect to each other. The reference clock rising edge and the rising-edges of even inverter outputs are transformed into short pulses using pulse generators (PG – Fig. 1(b)). The pulses generated from inverter outputs symbolize a specific (reference) instance in time during a single clock cycle and provide 16 functional and equally distant time references. A voltage-to-time converter (Section 5) creates an input pulse ($V_{in,pulse}$) which is delayed in time according to the ADC's analog input voltage. The timing of the input pulse is compared to the timings of the reference pulses by a set of dynamic (precharged)

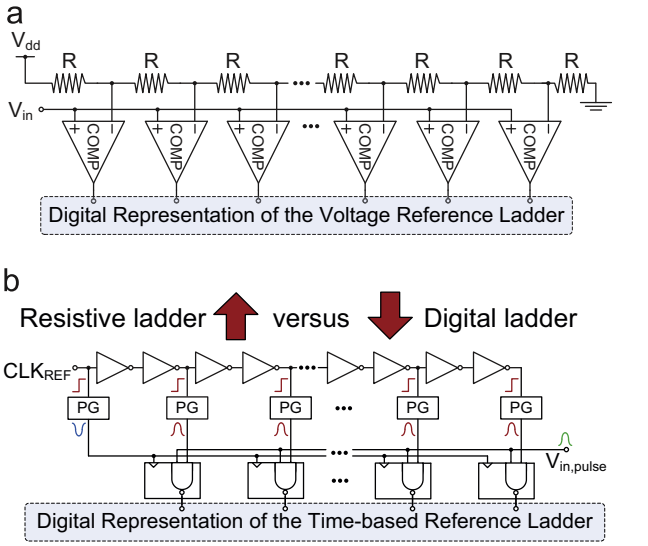

Fig. 1. Conventional (voltage-mode) reference ladder (a), and proposed digital (time-domain) reference ladder (b).

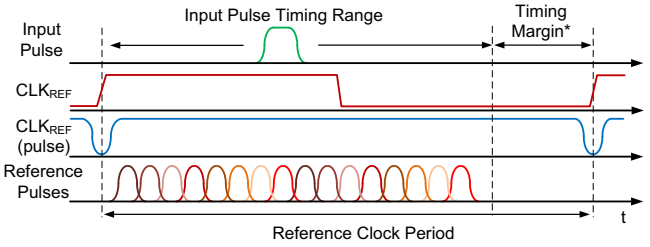

Fig. 2. Operation principle of the digital (time-domain) reference ladder ∗ timing margin is needed to account for PVT variations and to accommodate for the sampling time of the next input sample.

NAND-latches (time-domain comparators). A clock reference pulse ($CLK_{REF,pulse}$) is generated from the CLK_{REF} and used to precharge the NAND-latches. The operation principle of the new (time-domain) reference ladder is shown in Fig. 2. A set of reference pulses is generated during each reference clock period. Each of these pulses defines a different time reference and is provided to the input of a corresponding NAND-latch (Fig. 1(b)). The input pulse is provided to the remaining input of each NAND-latch. The digital signal value at the output of the latches changes depending on the timing of the input pulse compared to the reference pulses. Only the latches that receive a reference pulse which is close (in time) to the input pulse will provide a logic zero at the output. The location of zeros in the output code provides information about the input pulse position and therefore about the ADC's input analog voltage. Before the next rising edge of the reference clock, a timing margin is required (Fig. 2). This timing margin is necessary to account for the worst case PVT variations and at the same time accommodate enough time for correct input voltage settling and sampling. Because the reference delays can vary, the margin has to be large enough to deal with the worst-case delays (the PVT variations are calibrated at the converter input – see Section 5). The margin also needs to be large enough to enable sampling of the next input sample. The sampling pulse width is controlled by the delay between the input signal sampling clock (CLK_{SMPL}) and reference clock CLK_{REF} (see also Figs. 3 and 8). Because the CLK_{SMPL} rising edge comes before the CLK_{REF} rising edge, this timing delay needs to be accounted for within the CLK_{REF} cycle.