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A RF front-end for DVB-SH based on current conveyors

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ABSTRACT

Inductors are used extensively in Radio Frequency Integrated Circuits to design matching networks, load circuits of voltage controlled oscillators, filters, mixers and many other RF circuits. However, on-chip inductors are large and cannot be ported easily from one process to the next. Due to modern CMOS scaling, inductorless RF design is rapidly becoming possible. In this paper a new methodology for designing the RF frontend necessary for the DVB-SH in a 90 nm CMOS technology based on the use current conveyors (CC) is presented. The RF frontend scheme is composed of a second generation CC (CCII) LNA with asymmetric input and output, an asymmetric to differential converter, and a passive differential mixer followed by two CCII transimpedance amplifiers to obtain a high gain conversion. Measurements show a conversion gain of 20.8 dB, a 14.5 dB noise figure, an input return loss (S11) of −14.3 dB and an output compression point of −3.9 dBm. This combination draws 28.4 mW from a ±1.2 V supply.

1. Introduction

Digital Video Broadcasting-Satellite to Handhelds (DVB-SH) is a hybrid satellite/terrestrial system. It provides an efficient way of carrying multimedia services over hybrid satellite and terrestrial networks at frequencies below 3 GHz to a variety of mobile and fixed terminals having compact antennas with very limited directivity. Target terminals include handheld (PDAs, smartphones, etc.), vehicle-mounted, traveling, and stationary terminals. The satellite is used to cover large areas and, in places where there is no satellite coverage, terrestrial transmission is used [1–4].

In the design of Radio Frequency Integrated Circuits (RFIC), inductors are extensively used to design matching networks, load circuits of voltage controlled oscillators, filters, mixers and many other RF circuits. However, on-chip inductors are large and cannot be ported easily from one process to the next. Due to modern CMOS scaling, inductorless RF design is rapidly becoming possible. In this paper we describe a new methodology for designing the RF frontend necessary for the DVB-SH based on the use current conveyors (CC). This kind of circuits exhibit higher linearity, wider dynamic range and better high frequency performance compared to their voltage mode counterparts, operational amplifiers (OA). For these reasons, in recent years, CC circuits have received much attention for their use as RF basic building elements [5,6].

This paper deals with the design of the RF front-end for a DVB-SH receiver (2.17–2.20 GHz) using CC as the main building block. The paper is organized as follows. After presenting the front-end specifications and system architecture in Section 2, in Section 3 the principle of operation and some RF applications of CC will be discussed. Then, in Section 4 the RF front-end that includes a low-noise amplifier, an asymmetric to differential converter and a quadrature mixer will be explained. Measurement results will be presented in Section 5 and conclusion will be discussed afterwards.

2. DVB-SH analysis

A direct conversion receiver architecture (zero-IF) was chosen for this work. Fig. 1 shows the direct conversion receiver block diagram where the local oscillator (LO) frequency is equal to the input carrier frequency (2.17–2.2 GHz). Note that channel selection requires only a low pass filter with relative sharp cut-off characteristics.

This architecture has several issues. First, in a direct conversion topology, the down converted band extends to zero frequency. As a result, offset voltages can corrupt the signal and saturate the following stages. This issue is also related to the LO leakage because the LO radiation could appear as a DC voltage at the receiver output. Second, phase and frequency modulation requires shifting either RF or LO signal output by 90°. This shifting generally introduces errors and noise. Due to this error I/Q mismatches could appear, thereby raising the bit error rate. Third, in baseband, the even-order harmonics could be into the desired channel. Fourth, due to the desired

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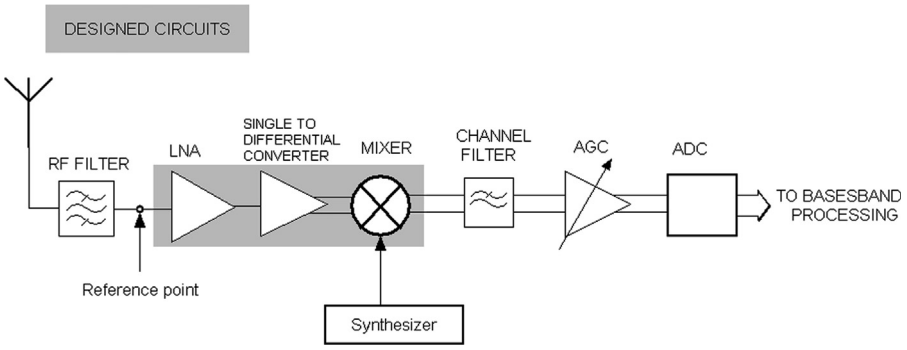

Fig. 1. DVB-SH receiver.

channel is translated directly to baseband, the flicker noise could affect the signal.

On the contrary, the simplicity of the direct conversion architecture offers two important advantages. First, the problem of the image frequency does not appear and no image filter is required. Second, the IF-SAW filter and other down-conversion stages, used for instance in heterodyne receivers, are replaced with low-pass filters and baseband amplifiers, so this architecture is more suitable for a monolithic integration with a relatively low area and low power consumption.

The receiver performance is defined according to the reference point shown in Fig. 1. The downlink frequency for the S bands of the DVB-SH standard was assigned between 2170 MHz and 2200 MHz [1]. The minimum required carry to noise by the system is −3.9 dBm [1]. The maximum input level at the antenna is −28 dBm [7] which means −29.5 dBm at the reference point (the IF-SAW filter insertion loss is 1.5 dB).

According to [7], the total noise figure and the minimum detectable signal of the RF front-end at the reference point are 3 dB and −112.55 dBm, respectively. The dynamic range of the receiver can be calculated as follows:

$$\text{Dynamic range} = P_{\text{inmax}} - P_{\text{inmin}} \tag{1}$$

where $P_{\text{in max}}$ is the maximum input level at the reference point and $P_{\text{in min}}$ is minimum detectable signal at the reference point. Thus, the dynamic range of the RF front-end is

$$\text{Dynamic range} = -29.5\ \text{dBm} - (-112.55\ \text{dBm}) = 83.05\ \text{dB} \tag{2}$$

The rail-to-rail voltage of the analog to digital converter (ADC) used is 1 Vpp, what means that the maximum allowed input power to the ADC (P_{max}) is:

$$P_{\text{max}} = 10\log\left(\frac{\text{Vpp}}{2\sqrt{2}}\right)^2 = -9\ \text{dBV} \overset{Z=50\ \Omega}{\Longrightarrow} P_{\text{max}} = 4\ \text{dBm} \tag{3}$$

The maximum gain (G_{max}), required by the front-end, can be obtained by fixing the noise floor of the receiver just above the Nyquist noise (N_{Q}) of the ADC. In this case, the ADC used has 70 dB of signal-to-noise ratio (SNR), so

$$N_{\text{Q}} = P_{\text{max}} - \text{SNR} = 4 - 70 = -66\ \text{dBm} \tag{4}$$

and the maximum gain is calculated as

$$G_{\text{max}} = N_{\text{Q}} - \text{P}_{\text{in min}} = -66 - (-112.55) = 46.55\ \text{dB} \tag{5}$$

To obtain the minimum gain (G_{min}) required by the system the condition of non-saturation of the ADC was fixed. For this reason, the maximum output power of the front-end must be below the maximum input power of the ADC. Thus

$$G_{\text{min}} = P_{\text{in max ADC}} - P_{\text{in max front-end}} = 4 - (-29.5) - 6 = 27.5\ \text{dB} \tag{6}$$

where the margin of 6 dB has been added as a back-off to prevent the saturation of the ADC.

Table 1
RF frontend specifications.

Receiver architecture	Zero-IF
RF frequency (GHz)	2.17–2.2
Sensitivity (dBm)	−112.55
Noise figure (dB)	3
Maximum gain (dB)	46.55
Dynamic range (dB)	83.05
Maximum input level (dBm)	−29.5
Channel bandwidth (MHz)	8
IIP3 (dBm)	−0.175
ACS (dB)	60

Finally, the dynamic gain is calculated as the difference between the maximum and minimum gain values previously calculated:

$$\text{Dynamic gain} = G_{\text{max}} - G_{\text{min}} = 46.55 - 27.5 = 19.05\ \text{dB} \tag{7}$$

The third order input interception point can be calculated by means of the third order inter-modulation products as follows:

$$\text{IIP3} = \frac{I_{\text{MD3}}}{2} + P_{\text{in}} \tag{8}$$

where the I_{MD3} is the intermodulation distortion from the third order of a circuit. The obtained IIP3 is −0.175 dBm according to [7]. The Adjacent Channel Selectivity (ACS) of a DVB-SH receiver must be at least 50 dB for an adjacent channel of 5 MHz and 60 dB for an adjacent channel of 10 MHz [1]. To finish this section, in Table 1 a summary of RF receiver specifications for the DVB-SH is presented.

3. Current conveyor principle of operation

This paper proposes the use of current conveyors (CC) to implement the DVB-SH RF front-end. Current conveyors [8] are active elements with three ports, *X*, *Y* and *Z*, described by (9):

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{pmatrix} \cdot \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix} \tag{9}$$

where b characterizes the current transfer from *X* to *Z*. For $a=1$, the circuit is a first generation current conveyor (CCI). It is called a second generation current conveyor (CCII) for $a=0$, and for $a=-1$ the circuit is called third generation current conveyor (CCIII) [9]. With $a=0$ and $b=1$, they have unity gain and

$$V_X = V_Y \tag{10}$$

$$I_Z = I_X. \tag{11}$$

Since its first introduction by Sedra and Smith in 1970 [8], current conveyors have been used as building blocks for analog