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Transimpedance amplifier with a compression stage for wide dynamic range optical applications

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ABSTRACT

A high dynamic input transimpedance amplifier was implemented in 130 nm CMOS technology. The proposed TIA is an inverter with a diode connected NMOS and a gate controlled PMOS loads which is cascode connected with the inverter. The square law compression NMOS increases the input photocurrent up to 10 mA. The TIA has an integrated input referred noise current of 135 nA, 227 MHz bandwidth. The TIA shows a transimpedance gain of 59 dBΩ and a 97 dB dynamic range. The TIA consumes 2.3 mA from 1.5 V voltage supply.

1. Introduction

The optical receivers used to monitor the laser optical power and in distance measurement experience high input optical power variations. The minimum received optical power varies from fractions micro-watts to several micro-watts; depending on the laser optical power and the maximum distance to be measured. The frequency range of the transmitted and received signals starts from 1 MHz up to hundreds of MHz depending on the required accuracy and the minimum distance to be measured. For higher accuracy and smaller measurable minimum distance, a higher bandwidth optical receiver with hundreds of MHz is required. A typical example of using 104 MHz optical signal to measure a distance up to 10 m with and accuracy of 6 mm, and achieved minimum distance of 30 cm, using 1 W laser power [1].

The dynamic range (DR) of the received optical signal in these applications can be as high as 6 decades. For high input optical power the conventional linear TIA can easily saturate and works improbably. The dynamic range is the working range for the TIA for the input optical power going from its minimum (sensitivity at certain BER) to its maximum input optical power (overload optical power), which is limited by TIA saturation. The dynamic range can be increased by increasing the sensitivity (TIA with lower noise) and/or increasing the maximum received input optical power where the TIA reaches saturation. The maximum limit can be increased by using a TIA with AGC or gain compression stage [2,3]. Fig. 1 illustrates the region of operations for a TIA with compression stage. For small photocurrent less than the break point $I_{in,B}$, the output voltage rises linearly with the small input current. If there is not a compression stage the TIA will saturate at low input current level $I_{in,sat}$. By using a compression stage, as the input current increases further above $I_{in,B}$, the output voltage is compressed and rises very slowly with the input current up to $I_{in,max}$. As a result the input current is extended from $I_{in,sat}$ to $I_{in,max}$.

A 240 MHz bandwidth 112 dB DR TIA was implemented in 0.6 μm SiGe BiCMOS technology introduced in [4]. The compression technique is a logarithmic one based on the exponential relation between BJT current and base-emitter voltage. The SiGe technology has a higher intrinsic gain and transit frequency compared to its counter CMOS technology but it is more expensive, also the BJT high power consumption in the front-end is an issue.

A TIA circuit based on square root compression is introduced in [5] using 40 nm CMOS technology. The TIA consists of a fixed feedback resistor across a three-stage voltage amplifier: inverter at the input and two common-source (CS) stages. A cascode inverter used as first stage as it gives higher gain than the CS and conventional inverter. The high gain was achieved by three stages TIA with reduced stability and higher power consumption. The instability is an important issue to be considered in this design due to multistage TIA.

The logarithmic compression introduced in [6] using 0.5 μm CMOS technology, demonstrates operation with currents ranging seven orders of magnitude from 200 fA to 2 μA with a limited bandwidth of 5 kHz. The logarithmic compression is achieved by MOSFET operation in sub-threshold region.

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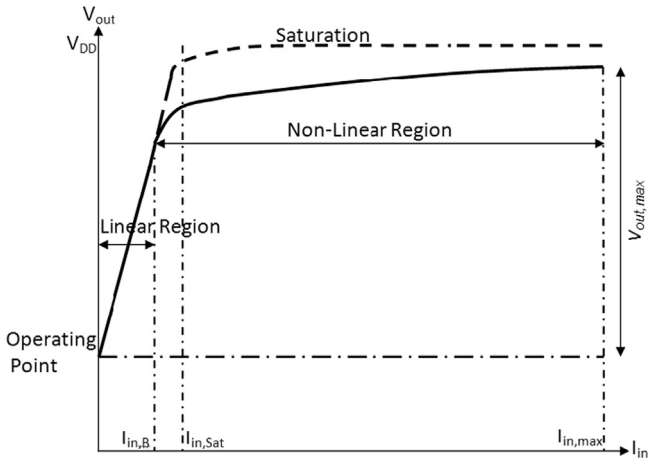

Fig. 1. Regions of operations for the input-current compression TIA.

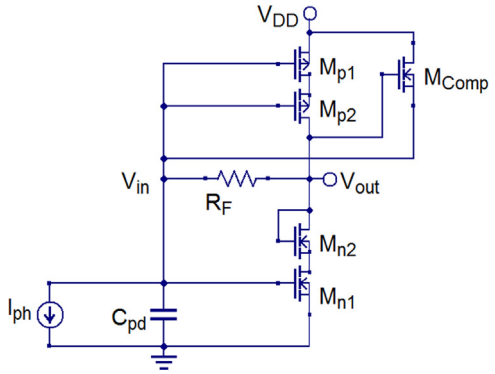

Fig. 2. Transimpedance amplifier with compression stage and stability compensation.

The TIA proposed in [7] displays a maximum transimpedance gain of 88.3 dBΩ with the −3 dB bandwidth of 1.8 GHz using 1 pF photodiode capacitance, exhibits an input current dynamic range from 100 nA to 10 mA. The circuit is fabricated using an 180 nm CMOS process and dissipates a dc power of 9.4 mW with 1.8 V supply voltage.

In this paper a wide dynamic range TIA with a compression stage will be introduced. The TIA stability will be ensured by introducing a load with controlled resistance. The new TIA compression and stability circuitry is implemented in 130 nm CMOS technology and the results will be introduced and discussed in the last section.

2. Transimpedance amplifier circuitry with compression stage

The proposed TIA uses shunt-shunt feedback (R_F) across an inverting voltage amplifier, see Fig. 2. The inverter voltage amplifier (M_{n1}, M_{p1}) has a gate controlled PMOS M_{p2} and diode connected NMOS M_{n2} loads. The inverter will give high voltage gain due to the higher total transconductance $G_m = g_{mn1} + g_{mp1}$. The cascode like connected MOSFETs (M_{n2} and M_{p2}) will increase the voltage gain of the amplifier.

The compression MOSFET M_{Comp} is OFF at low input photocurrent. As the input photocurrent increases M_{Comp} starts to conduct, it makes a second path for the input current. V_{gs} of M_{Comp} is equal to the voltage drop across R_F, as the input current increase the voltage drop across R_F increases and M_{Comp} start to conduct.

This makes a second path with controlled resistance for the input photocurrent. As the input current increases the voltage across V_{gs} of M_{Comp} increases and its resistance will decreases, and more photocurrent will pass through M_{Comp}. This will reduce the voltage drop across R_F to extend the right region of operation and prevent the TIA saturation at high input current levels.

From the small signal model, at low input photocurrents, the transimpedance gain can be approximated by the following expression:

$$Z_T(s) = \frac{\frac{R_F \cdot A_{vc}}{1+A_{vc}}}{1+\frac{C_{in} \cdot R_F \cdot S}{1+A_{vc}}} \approx \frac{R_F}{1+\frac{C_{in} \cdot R_F \cdot S}{A_{vc}}} \quad (1)$$

The dominant pole of this structure is at the input node, so its bandwidth can be approximated as

$$BW = \frac{1+A_{vc}}{2\pi R_{FB} C_{in}} \quad (2)$$

The maximum transimpedance gain is given

$$Z_{Tmax} \approx R_F \quad (3)$$

At high input photocurrents the transimpedance gain is reduced to be

$$Z_{Tmin} \approx \left(\frac{R_{in}}{R_{in}+r_{Comp}}\right) \cdot R_{FB} \quad (4)$$

Where the input resistance of the TIA is

$$R_{in} = \frac{R_{FB}}{1+A_{vc}} \quad (5)$$

and the resistance of the M_{Comp} as a function of VGS is calculated by

$$r_{Comp} = \frac{1}{\lambda \cdot \left(\frac{W}{L}\right) \cdot \mu \cdot C_{ox} \cdot (V_{GS}-V_T)^2} \text{(works in saturation region)}$$

The voltage gain of the cascode inverter is

$$A_{vc} = \left(g_{m,n1}+g_{m,p1}\right).r_o = \left(g_{m,n1}+g_{m,p1}\right) \cdot \left[\left(g_{m,n2} \cdot r_{ds,n2} \cdot r_{ds,n1}\right) // \left(g_{m,p2} \cdot r_{ds,p2} \cdot r_{ds,p1}\right)\right] \quad (6)$$

where r_o is the cascode inverter stage output resistance and the total input capacitance is given by

$$C_{in} = C_{PD} + C_{ESD} + C_{PAD} + C_{gs,n1} + C_{gs,p1} + (C_{gd,n1} + C_{gd,p1}) \quad (7)$$

The miller effect is reduced due to the cascode configuration and the term $(1+A_v)(C_{gd,n1}+C_{gd,p1})$ in regular inverter is reduced to be only $(C_{gd,n1}+C_{gd,p1})$.

Fig. 3 illustrates the noise sources in the proposed CI-RGC TIA without M_{Comp}. The compression MOSFET M_{Comp} has no effect on the TIA sensitivity as it is OFF at low input current. At high input current the additional M_{Comp} noise is negligible compared to the high input current.

The total output noise voltage spectral density is the summation of R_F thermal noise and the cascode amplifier noise at the output node

$$\frac{\overline{v_{n,out}^2}}{\Delta f} = \overline{i_{n.R_F}^2}\left|Z_{T(S)}\right|^2 + \left(\overline{i_{n.Mn1}^2} + \overline{i_{n.Mp1}^2} + \overline{i_{n.Mn2}^2} + \overline{i_{n.Mp2}^2}\right)\left|Z_{O(S)}\right|^2 \quad (8)$$

The input referred noise current spectral density can be calculated by dividing the output noise voltage in Eq. (8) by the transimpedance gain $|Z_{T(S)}|^2$ in Eq. (1)

$$\frac{\overline{i_{n.in}^2}}{\Delta f} = \frac{\frac{\overline{v_{n,out}^2}}{\Delta f}}{\left|Z_{T(S)}\right|^2} \quad (9)$$