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A low phase noise and low spur PLL with auto frequency control circuit for L1-band GPS receiver

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ABSTRACT

A low phase noise and low spur phase-locked loop (PLL) for L1-band global positioning system receiver is proposed in this paper. For obtaining low phase noise for PLL, All-PMOS LC-VCO with varactor-smoothing technique and noise-filtering technique is adopted. To reduce the reference spur, a low current-mismatch charge pump is carefully designed. A quasi-closed-loop auto frequency control circuit is used to accelerate the lock process of PLL. The PLL is fabricated in 180 nm CMOS Mixed-Signal process while it operates under 1.8 V supply voltage. The measured output frequency of PLL is 1.571 GHz and output power is −1.418 dBm. The in-band phase noise is −98.1 dBc/Hz @ 100 kHz, while the out-band phase noise is −130.3 dBc/Hz @ 1 MHz. The reference spur is −75.8 dBc at 16.368 MHz offset. When quasi closed-loop AFC is working, the measured lock time is about 10.2 μs.

1. Introduction

The L1-band signal of global positioning system (GPS) is widely used in the field of civil navigation. GPS receiver must have low noise figure to obtain accurate position information from weak satellite signal of L1-band. Regarded as an essential building block, phase-locked loop (PLL) is usually used to generate local oscillation signal in GPS radio front-end. However, the IF signals spectrum in GPS radio front-end may be corrupted by the spur tones of PLL, while the carrier-to-noise density radio (C/N_0) may also be degraded by the phase noise of PLL [1]. As the phase noise of VCO is one of main noise sources for PLL, a low phase noise VCO must be designed. All-PMOS topology and noise-filtering technique are adopted in the VCO structure. The tuning sensitivity (K_{VCO}) is another important parameter for the phase noise of VCO. When K_{VCO} is large, phase noise of VCO may deteriorate due to the AM–FM modulation [2]. To reduce K_{VCO}, a small size varactor is adopted. However the nonlinearity of varactor still makes K_{VCO} change sharply inside the voltage control range and degrades essential PLL features like phase noise [3]. So the varactor-smoothing technique is adopted to equalize K_{VCO}. Reference spur of PLL is concerned with non-idealities of the charge-pump (CP) [4]. Non-idealities of the phase frequency detector (PFD) and CP can be partly solved by time-delay technique and low current-mismatch technique.

A switch-capacitor array bank is adopted to cover the desired frequency tuning range in low K_{VCO} condition. The automatic frequency calibration circuit (AFC) can find optimum frequency control code and ensure VCO to operate in the appropriate frequency sub-band. Reported methods for AFC can be categorized into open-loop type and closed-loop type [5]. In typical open-loop method, counters are used to compare the frequency of divided VCO signal with a reference signal. Whole process of counting may take long time [6]. The closed-loop AFC method is always chosen for its simplicity. However, the lock process of closed-loop AFC may still take long time because the loop setting time depends on the loop design parameters such as loop bandwidth and initial value of control voltage [7]. Therefore, a quasi-closed-loop AFC method is proposed to accelerate calibration process.

In this paper, a low phase noise and low spur PLL with AFC is designed for L1-band GPS receiver. First, the detailed design parameters of PLL are calculated. Secondly a low phase noise VCO, a prescaler, a output buffer for test and a divider 96 are described. To shorten the lock time of PLL, the quasi-closed-loop AFC method is used. Additionally, phase-frequency detector with delay chain and low current-mismatch charge pump are designed to reduce the reference spur. Finally, PLL is implemented in a 180 nm CMOS Mixed-Signal process and measurements of chip are shown.

2. Circuit implementation

2.1. Design parameters of PLL

The block diagram of the proposed PLL is shown in Fig. 1. It mainly includes a PFD, a CP, an out-chip three-order passive loop

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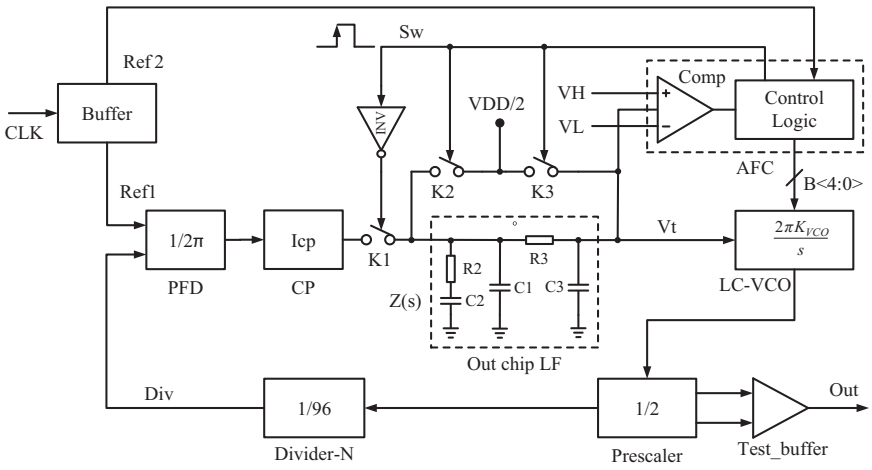

Fig. 1. Block diagram of the proposed PLL.

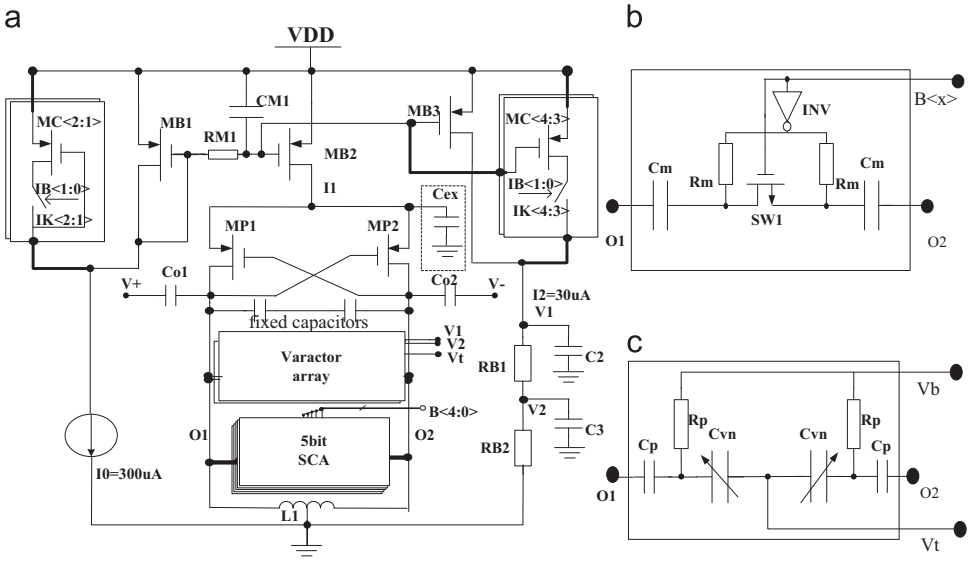

Fig. 2. The schematic of (a) LC-VCO, (b) one branch of 5 bit SCA, and (c) one branch of varactor array.

filter (3rd-LF),a low phase noise LC-Tank voltage-controlled oscillators (LC-VCO), a prescaler, an output buffer for test (Test_buffer), a integer divider-N and an AFC circuit. A temperature compensated crystal oscillator (TCXO) generates reference clock signals 'Ref1' and 'Ref2'.PFD detects phase error between reference clock signals 'Ref1' and the feedback signals 'Div'. The phase error is sent to the CP and corresponding current pulses are filtered by out chip LF to control the VCO's frequency. Half of VCO's output frequency is obtained by a prescaler and is amplified by Test_buffer. In the AFC circuit, V_t is compared with a specific voltage range (from VL to VH). Control logic circuit generates control bits $B\langle 4{:}0\rangle$ and switch control signals Sw for three switches (K1–K3).

The working process of PLL in Fig. 1 can be divided into two stages: the coarse frequency band searching process (AFC process) and the fine frequency and phase locking process (lock process). In near lock condition, the open-loop transfer function $T(s)|_{open}$[1] of the PLL can be obtained [8]

$$T(s)|_{open} = \frac{I_{cp}}{2\pi}\frac{2\pi K_{VCO}}{s}\frac{1}{2N}Z(s) \tag{1}$$

In Fig. 1, the impedance $Z(s)$ of the 3rd-LF is

$$Z(s) = \frac{1+s/\omega_z}{C_T s(1+s/\omega_{p1})(1+s/\omega_{p2})} \tag{2}$$

where $\omega_z = 2\pi f_z$ is the zero angular frequency,$C_T = C_1+C_2+C_3$ is total capacitance, $\omega_{p1} = 2\pi f_{p1}$ and $\omega_{p2} = 2\pi f_{p2}$ is the first and second pole angular frequency, respectively.Comparing the second-order loop filter (2nd-LF), additional pole in the 3rd-LF can provide extra attenuation A_t for reference spur [8]. To ensure loop stability, ω_{p2} should be equal to or greater than ω_{p1} while C_3 should be smaller than $C_1/10$. By setting the 2nd-LF's loop bandwidth $\omega_{c2} = 2\pi f_{c2}$, phase margin PM and additional attenuation A_t, The 3rd-LF's zero angular frequency ω_z, two pole angular frequency ω_{p1} and ω_{p2}, loop bandwidth $\omega_{c3} = 2\pi f_{c3}$ can be obtained:

$$\omega_{p1} \approx \frac{\omega_{c2}}{\sec(PM) - \tan(PM)} = \frac{C_T}{R_2 C_2 C_1} \tag{3}$$

[1] In the strict sense, the z-domain transfer function is used for charge pump PLL. But the s-domain model can be used for charge pump PLL under the condition that loop bandwidth is smaller than one-tenth of the input reference clock.