Microelectronics Journal 45 (2014) 1118–1124

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Nanoelectronic content-addressable memory

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ARTICLE INFO

Article history:
Received 12 February 2013
Received in revised form
6 May 2014
Accepted 12 May 2014
Available online 24 June 2014

Keywords:
Logic circuits
Memory
Nanoelectronic
Neural network
Single-electron

ABSTRACT

A novel nanoelectronic single-electron content addressable memory is designed and simulated. The proposed memory has three important building blocks: a storage block, a comparison block and an addressing block. These building blocks were built based on single-electron circuits such as Reset-Set latches, exclusive-or gates and a WTA neural network. Each one of the building blocks was separately adjusted to provide room temperature operation before being connected together. Some analyses concerning stability of each block and of the whole memory circuit were made. The nanoelectronic memory was successfully validated by simulation.

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1. Introduction

Single-electron tunnelling devices (SET) may become an extremely attractive option for the development of giga (GSI) and tera (TSI) scaled integrated circuits. Low power consumption, reduced dimensions and fast operation are pointed as some of its benefits, which also include low noise behaviour and an excellent current control.

Many single-electron devices have already been proposed [1–6], especially in the logic gate field. Some of these proposals only replace conventional CMOS for SET devices [7]. Nevertheless, there are two critical points in this kind of strategy. The first one is that the operation of single-electron circuits is not deterministic since the major charge transport mechanism is tunnelling, which is a probabilistic phenomenon. The second one is the presence of random background charges which may degrade the circuit's operation. To overcome these limitations, one possible strategy is to develop new architectures for SET circuits.

In previous works, studies of nanoscale memory devices have been made [8] and single-electron memory circuits were proposed. Yamanaka et al. [9] proposed a stochastic associative memory by using a unit SET model combined with MOS structures and Degawa et al. [10] proposed a content-addressable memory constituted of hybrid SET-MOS circuits. In addition, Yano et al. [11] proposed a single-electron memory in which information can be read and write using SET-MOS devices. None of these proposals were entirely designed for single-electron applications and MOS devices were also required.

Furthermore, Wasshuber et al. [12] gave some examples of memory cells which can just be individually used for simple storage applications and Karafyllidis et al. [13] presented a single-electron RAM without making any considerations of its behaviour at room temperature. Finally, Carmo et al. [14] proposed a stochastic associative memory fully implemented with single-electron devices. In this proposal, the maximum operating temperature did not reach room temperature and no considerations of enhancing its value were made.

The architecture of a new single-electron content-addressable memory was designed to overcome these limitations. First, several single-electron logic circuits proposed in literature [1,2,3,4,7,12] were investigated at 300 K and in the presence of random background charges by simulation. After that, their performances were compared in order to identify which devices behaved properly under these conditions. Finally, the fully implemented SET memory, which may operate at room temperature, was proposed.

This paper is organised as follows. Section 2 introduces the single-electron content-addressable memory architecture and presents its corresponding memory, comparison and addressing blocks. Section 3 describes the performance of the proposed memory. Finally, the conclusions are presented in Section 4.

2. The nanoelectronic memory architecture

The block diagram of the proposed single-electron content-addressable memory circuit, hereinafter referred as SET-CAM, is

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http://dx.doi.org/10.1016/j.mejo.2014.05.022
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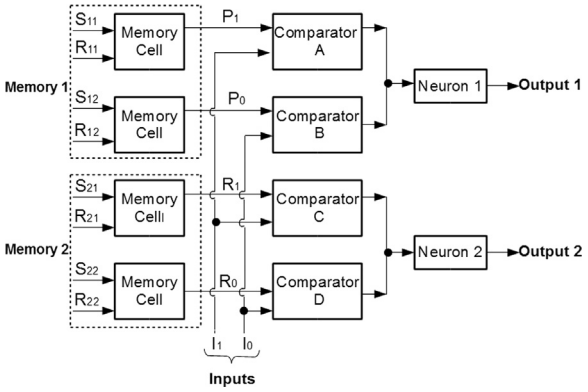

Fig. 1. Block diagram of the proposed single-electron content-addressable memory.

shown in Fig. 1. As a digital circuit, the information carried among its topology is associated to the binary unity/zero code, which is represented by the presence or absence of one or a small group of electrons in the island. This operation principle, based on the Coulomb Blockade effect, is commonly used on single-electron logic devices.

It is known that a content-addressable memory addresses the circuit's output according to the result of operations such as comparison between entries and stored values [15]. In order to obtain the expected operation of a CAM, the proposed circuit on its topology includes memory cells, comparison devices and neural networks which identify the winner address among the others. The proposed SET-CAM is presented on its simplest form, with the storage and comparison of two-bit words. The input word, whose bits are called (I1,I0), is compared to the first stored word (P1,P0) and to the second stored word (R1,R0).

According to the similarity of the compared words, the memory addresses its content. If there is a perfect match, *i.e.* if a stored word is similar to the input word, its corresponding address is identified as a winner by the memory circuit and its output voltage assumes the logic level 1. On the other hand, if there is no match with the searched word, the circuit identifies the winner based on bit-matches. Therefore, the word that has more similar bits compared to the bits of the searched word, considering its significance, is considered winner.

The behaviour of the proposed SET-CAM described before is summarised in Table 1, when the input word is made (0,0). The other cases, which will be here omitted, can be obtained directly from the circuit operation. It is important to say that, in Table 1, "*x*" represents the logic "do not care". Moreover, notice that when the same word is stored, the circuit is incapable of determining a winner.

In the proposed SET-CAM circuit, the single-electron memory cell will be represented by a Reset-Set latch. Furthermore, the interconnection of exclusive-or gates will constitute the comparison block of the designed SET-CAM while the neural network in the modified winner-take-all configuration will identify the winner word. A detailed approach of each circuit block will be described in the following sections.

2.1. Storage block

The Reset-Set latch is commonly used on memory devices because of its capability of writing, storing and erasing data. On the proposed SET-CAM circuit specifically, this logic device will be used to storage words, represented by the bits (P1, P0, R1, R0).

The stored bits, on the other hand, will be obtained from the association of set and reset entries of memory cells, indicated in Fig. 1 as S11, R11, S12, R12, S21, R21, S22 and R22. Consequently,

Table 1
Behaviour of the proposed SET-CAM when the Input word is equal to (0,0).

Input word (I1,I0)	Stored word 1 (P1,P0)	Stored word 2 (R1,R0)	Output
(0,0)	(P1,P0)	(P1,P0)	–
	(0,0)	(*x*,1)	Stored word 1
	(0,0)	(1,*x*)	Stored word 1
	(*x*,1)	(0,0)	Stored word 2
	(1,*x*)	(0,0)	Stored word 2
	(0,1)	(1,0)	Stored word 1
	(0,1)	(1,1)	Stored word 1
	(1,0)	(0,1)	Stored word 2
	(1,0)	(1,1)	Stored word 1
	(1,1)	(0,1)	Stored word 2
	(1,1)	(1,0)	Stored word 2

Table 2
Logic truth table of a reset-set.

SET Input	RESET Input	Output (Q_{n+1})
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

the operation of this memory block is represented by the classical logic truth table of a Reset-Set latch for each stored bit, which is shown in Table 2.

The topology of the memory device here used was proposed by Lageweg et al. [3]. It is important to say that this Reset-Set latch is fully constituted of single-electron devices, which includes single-electron transistors and tunnel-junctions. Besides that, resistances, capacitances and voltage/current sources are also used.

The performance of the circuit was evaluated with the nanoelectronic simulator SIMON (Simulation of nano-structures) [16]. By using the suggested values on [3] for each device, it was obtained the expected behaviour at a maximum operating temperature of 1 K. However, it is desirable to obtain room temperature operation for the SET-CAM circuit, which means that each block of the content-addressable memory should operate individually at room temperature too.

In order to obtain the latch operation at 300 K, its devices were redesigned respecting the relationship between the electrostatic and thermal energy. The condition given by (1) was guaranteed to make tunnelling the major charge transport through the circuit. Besides that, the relationship between the charge of a node, its equivalent capacitance and voltage ($Q=CV$) was also observed.

$$Ec = \frac{e^2}{2C_{eq}} \gg k_B T \tag{1}$$

In formula (1), Ec is the charging energy, e is the elementary charge, C_{eq} is the total capacitance around the island, k_B the Boltzmann constant and T is the temperature of the process. This leads C_{eq} to values smaller than 10^{-16} F, and, for near room temperature operation, capacitances should be in the order of 10^{-19} F. As a result, the basic capacitance proposed by Lageweg et al. [3] assumed the value 0.01 aF instead of 1 aF originally proposed. In that way, the latch was able to operate correctly when simulated in SIMON [16] at room temperature. The Reset-Set latch circuit used for simulation is shown in Fig. 2.

2.2. Comparison block

The comparison block of the proposed SET-CAM is constituted of four two-input exclusive-or gates. Each of them is fully

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