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Low-power level converting flip-flop with a conditional clock technique in dual supply systems

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ABSTRACT

Clustered voltage scaling (CVS) is an effective way to reduce power consumption in digital integrated circuits. Level-converting flip-flops are the critical elements in the CVS scheme. In this paper a single edge implicit pulse-triggered level-converting flip-flop with a conditional clock technique (CC-LCFF) is proposed and proved to be suitable for use in low-power non-critical paths with Dual-VDD. CC-LCFF conditionally blocks the clock signal when the input data does not make any transition, so the redundant transitions of internal nodes are eliminated and the total power consumption is reduced. Based on the SMIC 65 nm technology, the post-layout simulation results show that the proposed CC-LCFF shows an improvement of 69.41–72.40% in power consumption and 23.36–47.73% in power-delay product (PDP) as compared with its counterparts.

1. Introduction

With the increase in the integration level of integrated circuits, power consumption becomes increasingly prominent in high performance microprocessors. Since the switching power is proportional to the square of the supply voltage and the static power is proportional to the supply voltage, reducing the supply voltage is an efficient way to reduce power consumption [1]. A Dual-VDD technique has been developed based on that [2].

In order properly to assign VDD to gates in a Dual-VDD system, the Cluster Voltage Scaling (CVS) scheme is usually adopted. It applies a high supply voltage (VDDH) in critical paths to ensure high performance and low supply voltage (VDDL) in non-critical paths to reduce power consumption [2]. Thus, the circuit has reduced power consumption without degrading performance. However, the PMOS transistor of the VDDH block cannot be shut off completely if it is directly driven by the output of the VDDL block. Therefore, a level-converting circuit is needed between these two blocks, which can convert VDDL-swing input to VDDH-swing output. In order to alleviate the delay overhead of the level-converting circuit, level conversion is usually integrated in the flip-flop, forming a level-converting flip-flop (LCFF). As the critical element in CVS, the characteristics of the LCFF have a sizeable impact on the performance of the circuit. Thus designing a high-performance LCFF becomes an important issue [3–10], and a novel low-power pulse-triggered LCFF is proposed in this paper.

The rest of the paper is organized as follows. Section 2 reviews some previously published pulse-triggered LCFFs. The proposed implicit pulse-triggered level-converting flip-flop with the conditional clock technique is discussed in Section 3. Section 4 shows simulation results and analysis for various LCFFs. Section 5 contains the conclusion.

2. Review of pulse-triggered LCFFs

Pulse-triggered LCFFs are characterized by a simple structure and small delay and are attracting considerable attention [4–10]. In this section, we will describe some published pulse-triggered LCFFs.

Fig. 1 illustrates the schematic diagram of pulsed half-latch level-converting flip-flop (PHL-LCFF) [5] (λ=30 nm, gates in dark black are driven by VDDL). PHL-LCFF uses an explicit pulse generator (I1–I5) that generates pulses at the rising edge of the clock to sample the input data into the latch (I7 and I8). Because the NMOS pass transistor N3 is driven by a low-swing voltage VDDL, the keeper inverter I8 that works at VDDH must not be too strong to allow the input data to be sampled into the latch. When the input D is "0", the voltage at node LC is VDDL-Vth, but the keeper inverter I8 must restore it to VDDH. This threshold voltage drop problem at node LC obviously increases power consumption and delay. Moreover, its explicit pulse generator is still working even when the input data remains the same, which also leads to unnecessary power consumption.

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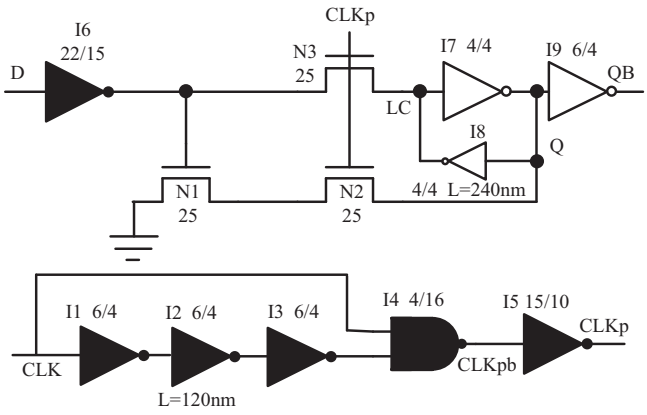

Fig. 1. Pulsed half-latch level converting flip-flop (PHL-LCFF).

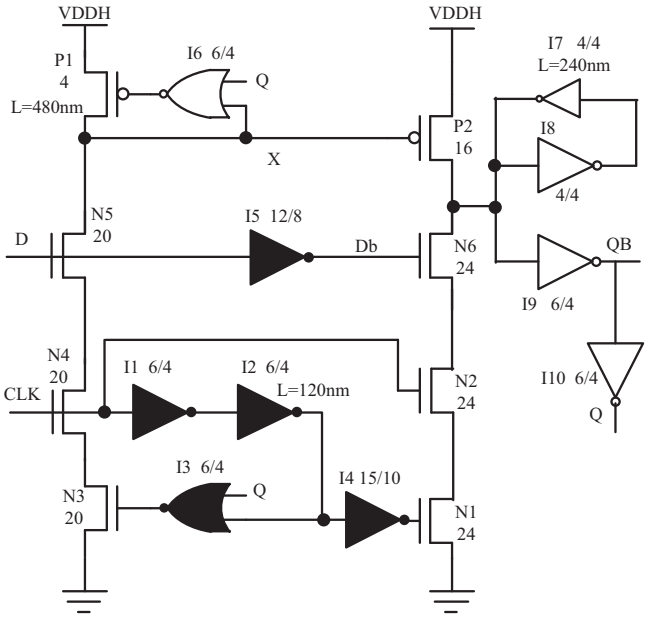

Fig. 2. Self-pre-charging level converting flip-flop (SP-LCFF).

A self-pre-charging level-converting flip-flop (SP-LCFF) is proposed in [6] and shown in Fig. 2. SP-LCFF uses the output Q to control the charge and discharge of node X. When Q is "1", the delayed clock signal is blocked by the NOR gate I3, so the discharging path (N3-N5) will not work. Meanwhile, NOR gate I6 outputs "0", and the node X is pre-charged to a high level by the PMOS transistor P1. The power consumption is reduced by elimination of the redundant discharge of X. However, the inverter chain (I1, I2 and I4) is still switching with the clock even when the input D does not make any transition, so the power consumption cannot be reduced efficiently.

A clocked pseudo-NMOS level converting flip-flop (CPN-LCFF) proposed in [10] is shown in Fig. 3, which is one of the most advanced single edge implicit pulse-triggered level converting flip-flops. An always-on PMOS transistor P1 is used to charge node X so that it will not float when the LCFF is idle. It adopts the feedback signal QF to eliminate the redundant discharge of node X. However, due to its implicit structure, there are too many stacked NMOS transistors in the discharging path (N3-N6) of node X. Since CLK and D are VDDL-swing signals, the widths of these NMOS transistors should be large enough to pull down the node X, which will increase the overhead of power and area. Moreover, its

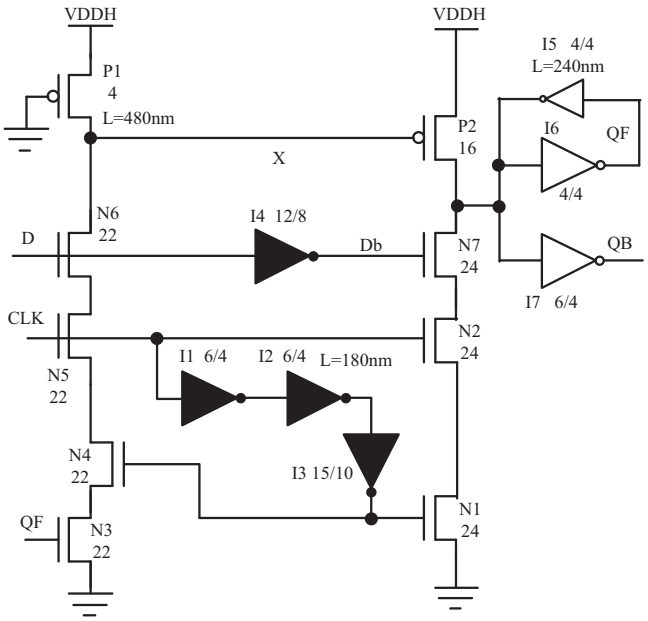

Fig. 3. Clocked pseudo-NMOS level converting flip-flop (CPN-LCFF).

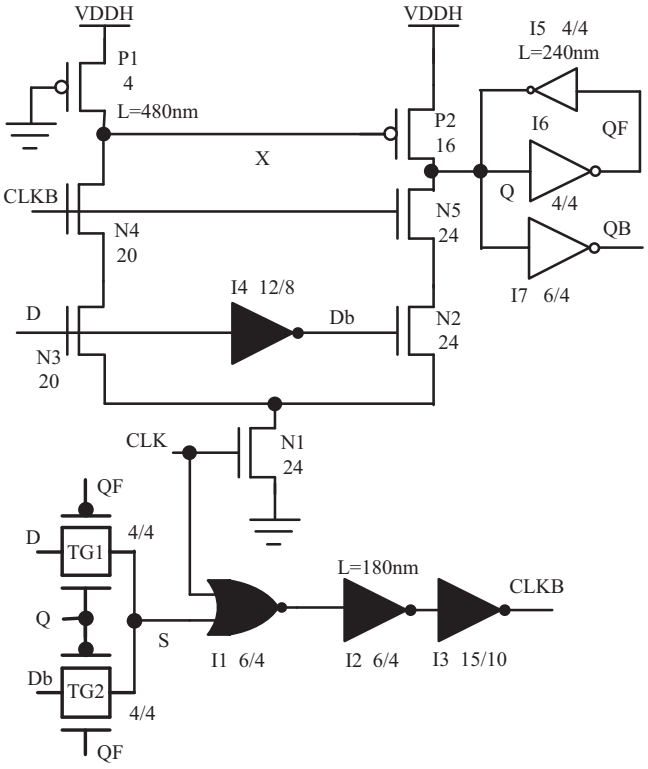

Fig. 4. The proposed level converting flip-flop with the conditional clock technique (CC-LCFF).

inverter chain (I1–I3) is still switching with the clock when the input D remains the same, in the same way as in the SP-LCFF.

3. The proposed LCFF with a conditional clock technique

As observed from the above pulse-triggered level-converting flip-flops, many internal nodes are still charged and discharged when the input remains unchanged in successive clock cycles, although some conditional capture techniques are adopted. The