Microelectronics Journal 45 (2014) 960–965

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Dedicated thermal emulator for analysis of thermal coupling in many-core processors

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ARTICLE INFO

Article history:
Received 19 August 2013
Received in revised form
20 December 2013
Accepted 2 January 2014
Available online 4 February 2014

Keywords:
ASIC
IC thermal modeling
Many-core processors
Power dissipation
Thermal analysis

ABSTRACT

This paper discusses the problem of thermal coupling in many-core processors manufactured in non-planar FinFET technologies. Our work focuses on two research goals. Firstly, the results obtained from the thermal simulations allow the investigation of mutual thermal influence between neighboring cores in such processors, what can be used to develop thermal models of such architectures. Secondly, we describe a test integrated circuit designed specifically to mimic the thermal behavior of microprocessors manufactured in various technologies. In particular, this paper describes its design and presents selected simulation results obtained using Green's function-based thermal software.

1. Introduction

Thermal analysis of integrated circuits is a crucial issue in modern multi-core processors with very small feature size, where thermal coupling between cores occurs. It will become even more important when the technology scales down and more cores are added on chip; some authors even expect processors with dozens or even hundreds of cores to be produced soon [1]. The constantly growing number of cores in the modern multi-core architectures is directly related with the demand for more and more computational power. This in turn provokes the increase of power density inside the chip. The heat has to be dissipated outside the integrated circuits in order to avoid physical damage which is especially important in modern technologies with high transistor densities. Research shows that temperature of a core significantly rises when it executes an intensive workload [2]. Due to shrinking distance between elements of modern microprocessors, an active core significantly affects the temperature in its neighborhood. This may lead to local hot spots and damaging the chip. It is foreseen that, in the future, special algorithms will be implemented which will allow distributing computation over cores that are not in close proximity in order to reduce thermal coupling between them.

Therefore, the research on new methodologies for fast and accurate thermal simulation of multicore processors is crucial and more and more research groups publish new approaches to this challenge [3]. In [4] authors proposed a composable model-based simulation for fast thermal design space exploration for multicore processors. In [5] a novel, adaptive chip-package thermal analysis technique for use in IC synthesis and design was presented. A simple thermal model used for estimating the temperature profiles for a multicore processor was shown in [6]. All these approaches are based on designing a fast yet accurate model which would allow the faster computation. However, in this paper we propose a different research direction. Instead of using a software simulator, our idea is to use a dedicated thermal chip emulator, which will not suffer from the performance/accuracy tradeoff. Our approach allows the simulator to run a cycle-accurate execution of various applications and dynamically compute the transient temperatures in every part of the chip within reasonable time. The main novelty of the proposed approach is the use of a custom-designed dedicated ASIC (*Application-Specific Integrated Circuit*), which serves a thermal emulator of a true multi-core processor.

The following section of this paper describes in detail the power modeling methodology. This is followed by the presentation of the test ASIC in Section 3. Next, the results of thermal simulations are discussed in Section 4. Finally, conclusions are provided in Section 5.

2. Power modeling

In our approach we considered an architecture based on the well-known Alpha21364 processor [7] scaled down to 20 nm and 10 nm technology nodes. Consequently, the simulated processor

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http://dx.doi.org/10.1016/j.mejo.2014.01.001

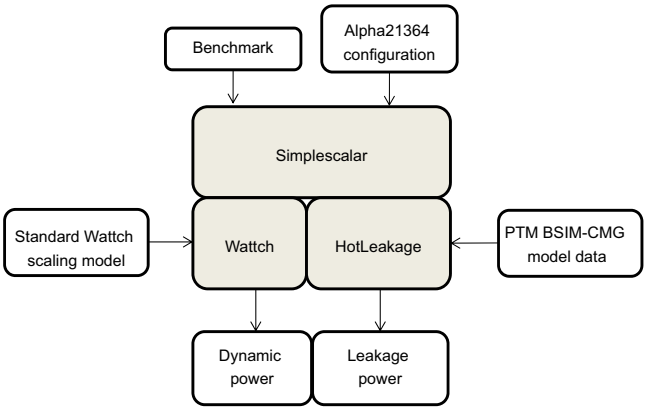

Fig. 1. Power modeling methodology.

parameters were configured according to those for the Alpha21364. The supply voltage was set to 0.9 V and 0.75 V for 20 nm and 10 nm technologies respectively. The power data for the scaled Alpha21364 chip is obtained using the well-known Wattch power model [8] integrated into the cycle-accurate performance simulator SimpleScalar [9]. The model parameters were calculated using the standard scaling method employed in many other publications [10,11]. Moreover, taking into account that in modern technologies leakage power is a major factor and it cannot be neglected, the leakage power was calculated in our model based on the HotLeakage tool [12]. The entire power modeling methodology is summarized in Fig. 1.

The inclusion of the new FinFET technologies required several enhancements to be made in the Wattch and HotLeakage tools. In order to estimate the parameters of leakage model for modern technologies, we performed the following steps. First, we ran the Cadence® Spectre circuit-level simulations of NMOS and PMOS transistors and calculated the leakage current for various temperature values and variable number of transistor fins. In the simulations we used the 20 nm and 10 nm PTM (*Predictive Technology Model*) [13], based on the recent BSIM-CMG model destined for multi-gate FETs. Then, the leakage current in function of temperature and the number of transistor fins was found. Next, an iterative procedure was applied to fit the leakage current data obtained from the HotLeakage model to the data from the Spectre program. Finally, after fitting all the functions, the estimated model parameters were included into the leakage model.

Taking into account that the HotLeakage allows only the calculation of leakage for memory-like structures, the leakage power for ALUs (*Arithmetic Logic Unit*) was only roughly estimated based on their area. The average power dissipated in Alpha21364 processor under heavy workload was estimated with the SimpleScalar tool executing various standard SPEC2000 benchmarks. In order to make sure that all the most computationally-intensive parts of each benchmark were executed the simulator is initially fast-forwarded several hundred million instructions and then several hundred million instructions are simulated with detailed power data statistics. In this way, the average dynamic and static power dissipation for every processor unit is estimated. A more detailed description of the power modeling methodology can be found in [14].

3. Asic design

3.1. Overview

The power trace data computed in the way described in the previous section may be used in thermal simulations of an ASIC, which is supposed to mimic the behavior of a microprocessor manufactured in different technologies. This section contains the description of the proposed ASIC. It is based on the experience gained during design of the circuit containing overlapping matrices of 9 heat sources and 25 diode temperature sensors. The detailed description of this work can be found in [16–19]. The new version of the ASIC was designed in the 0.35 μm CMOS high-voltage technology provided by austriamicrosystems® (AMS). This ASIC (more details can be found in [15]), sketched in Fig. 2, contains a large 16×24 matrix of transistor heat sources which can be individually switched on and off at a desired power level at a specified time instant. The dimensions of heat sources were chosen so that an integer or a floating point arithmetic unit in a real microprocessor would correspond in this circuit, as shown in the figure with the black squares, to a single heating cell in the 10 nm technology node and 4 cells in the 20 nm technology node. Similarly a 2 MB cache memory unit will correspond to 20 and 80 heating cells respectively. Owing to this solution it is possible to analyze thermal phenomena occurring in the state-of-the-art technologies experimenting with a circuit manufactured in a much older technology, which is much more cost effective. Using a dedicated ASIC for thermal simulation of modern ICs have been also proposed in [20]. Authors use however a different type of heat sources based on thin film resistors whereas in our chip power MOS transistors are implemented. Moreover, our ASIC has 384 heat cells, compared to 50 (10 heat sources for each of 5 layers) in the chip proposed in [20]. Therefore our chip can provide much more detailed results, while the other is rather dedicated for simulating 3D stacked architectures.

3.2. Heat cell details

The heating cell structure is based on current-mode devices. It comprises two current mirrors and a modified first-generation switched-current (SI) delay cell (see Fig. 3).

The operation principle is that the heater itself is a current mirror. The output transistor of this mirror is connected to high-voltage supply node. In order to provide high density of dissipated power the heater mirror is composed of NMOS transistor. All the

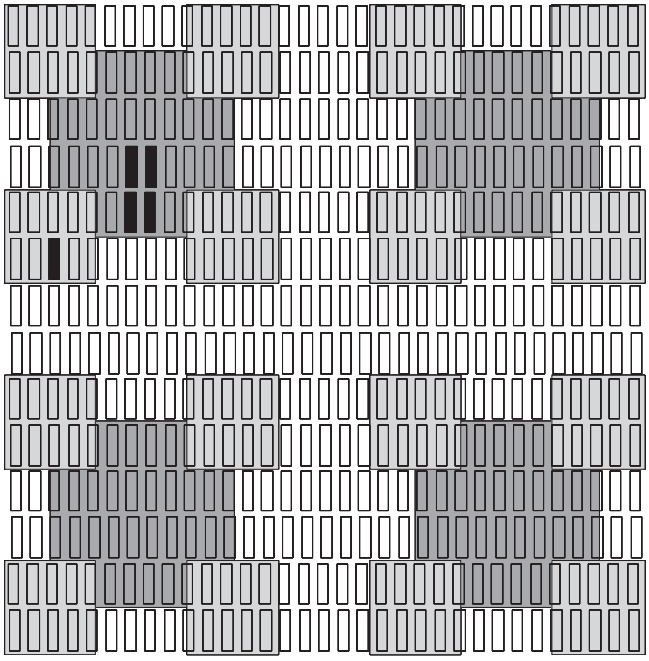

Fig. 2. Thermal test ASIC floorplan.