Microelectronics Journal 45 (2014) 491–499

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Electro-thermal high-level modeling of integrated circuits

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ARTICLE INFO

Article history:
Received 30 November 2012
Received in revised form
24 July 2013
Accepted 6 February 2014
Available online 17 March 2014

Keywords:
Electro-thermal
High-level model
3D IC
Verilog-A
VHDL-AMS
CAD

ABSTRACT

Operating temperature and temperature gradients are of critical concern in the design of planar integrated circuits (ICs) and are bound to be exacerbated in the upcoming 3D technologies. However, a thermal aware design of ICs allows thermal issues to be kept to the minimum. Previously, a simulator integrated in the Cadence® environment that allows electro-thermal simulations to be carried out at a transistor level has been presented. Since this simulator is based on the use of the Verilog – A® hardware description language, electrothermal simulation can be performed as long as high-level electro-thermal models are provided. In this paper, a methodology used to build such high-level electro-thermal models compliant with this simulator is detailed and simulation results at low and high level are compared.

1. Introduction

The operating temperature as well as the temperature distribution over integrated circuits (ICs) is a major issue. Indeed, an increase of delays in lines [1–3], power leakage, mismatches in analog circuits, thermal noise or mechanical stress are some of critical hindrances due to high operating temperatures [4–8]. In the upcoming 3D technologies such issues are bound to be ever more critical than in planar technologies [5,7,8]. If these issues cannot be totally avoided, it is at least possible to minimize them by optimizing the floor plan of ICs [5,7,9–11]. Therefore, it becomes necessary to take accurately the electro-thermal behavior of the IC into account from the early stages of the design flow.

In our previous works [12,13] a direct electro-thermal simulator developed for this purpose has been presented. Its operation principle consists in generating a thermal network representing the silicon die and its environment, i.e. the package, and to couple it to the electrical schematic of the circuit. For this purpose, the conventional electrical compact models of the devices (i.e. the transistors, resistances, etc.) are replaced by their electro-thermal counterparts. Those electro-thermal models have an additional terminal which is used to keep track of the temperature and to inject the heat flux generated by the device in the thermal network.

However, standard electrical simulations cannot be performed for LSI or VLSI systems at a transistor level. For such systems, simulations rely on electrical high level behavioral modeling [14,15]. This consists (i) in describing the electrical behavior between the different analog or digital ports of functional sub-circuits with a reduced set of equations and (ii) in simulating the resulting whole set of behavioral equations with a multi-domain solver such as SpectreS® or Eldo®. Although this high-level modeling and simulation concept is now well established for electrical simulations, no fast and efficient solution exists for the electro-thermal simulation of integrated systems. To our knowledge, all the developments in the field of electro-thermal simulation of integrated circuits addressed the issue at the transistor level for analog ICs [16–22] and at the gate level for digital ICs [16,23–25]. Thus, the size of the integrated system which can be simulated is limited. As for electrical simulations of VLSI systems, in order to be able to electro-thermally simulate huge integrated systems, the electro-thermal simulator has to rely on the use of behavioral languages for the description of the different functional sub-blocs of the system and electro-thermal high-level models of these sub-blocs have to be provided.

The electro-thermal simulator we developed and which has been already presented in [12,13], with a validation at the transistor level, relies on the use of the high-level behavioral Verilog-A language. It is thus compatible with high-level electro-thermal simulations. Its main features are briefly described in the next section. The main goal of this paper is to present how high-level electro-thermal models of analog functional blocs can be built and used with our electro-thermal simulator. The concept of high-level electro-thermal model and the proposed high-level modeling principle are thus described in Section 2, with three different modeling approaches which depend on the silicon surface occupied by the functional bloc to be modeled. In the fourth section, the high-level modeling of a proportional to absolute

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http://dx.doi.org/10.1016/j.mejo.2014.02.001
0026-2692

temperature (PTAT) sensor formerly presented and modeled at the transistor level in [13] is detailed as a case study. Then, before conclusion, the results obtained from the simulations at the transistor level of a test chip including 16 PTAT sensors are compared to the results obtained with two different high-level models of the sensor.

2. High-level electro-thermal simulation

Any electro-thermal simulator relies on the coupling of an electrical circuit network, aimed at modeling the electrical behavior of the integrated circuit to simulate, with a thermal network, aimed at modeling the way the heat generated by the components of the circuit is sunk to the ambient environment. These two networks have to be coupled in order to input the generated heat into the thermal network (electrical to thermal network coupling) and inversely to set the individual temperatures of the components (thermal to electrical coupling). When the thermal network is associated to a dedicated thermal solver, very often a F.E.M. solver, the electrical network is first solved with a SPICE-like circuit simulator which provides the thermal solver with the heat dissipated by each component of the circuit. The thermal simulation is thus performed to provide in return the temperatures of the components to the circuit simulator. The loop is then reiterated until the temperatures of the components remain stable. Both simulators are said coupled by relaxation [20,22]. It is a simple way to perform an electro-thermal simulation but the relaxation technique may exhibit convergence issues in circuits with a strong electro-thermal coupling [16,17]. Because of the well known analogy between thermal and electrical equations, the thermal network can be built as a RC network [12]. In this case, the thermal and electrical networks are directly coupled through specific thermal ports and the complete electro-thermal network is solved thanks to a circuit simulator. Here, the coupling is said direct and it has the advantage to ensure convergence whatever the electro-thermal coupling strength [16]. Our simulator [12,13] uses such a coupling and has been integrated into the Cadence® environment in order to benefit from the high-level behavioral language Verilog − A® and from the multi-domain solver Spectre®. As stated in the introduction, electro-thermal compact models are substituted for the conventional electrical compact models of the components, i.e. transistors and resistances. Each component now features an additional port, named a thermal port, which allows the coupling of the electrical and thermal sub-networks [12,13]. These electro-thermal compact models are written in Verilog − A®. Although the simulator has been experimentally validated through electro-thermal simulations performed at the transistor level [13], it is actually fully compatible with electro-thermal simulations at higher description levels, as long as high-level electro-thermal models are provided. A method to develop such high-level models is presented in this paper.

Whatever the level of the used electro-thermal models, the question which arises is how fine should be the thermal sub-network coupled to the electro-thermal sub-network. The electro-thermal sub-network is the conventional electrical network where each entity has at least one additional thermal port. Considering all the thermal ports of the components of the whole system, the natural way to build the thermal sub-network is to link all these thermal ports with equivalent thermal resistances and capacitances. However, in practice, building this way the thermal sub-network leads to high inaccuracy in the calculation of the thermal map over the chip. It means that the size of the thermal sub-network cannot be reduced the same way the electro-thermal sub-network is reduced by the use of lumped equivalent circuit models, i.e. the use of electro-thermal compact models of the components. Indeed, the heat goes in all the directions into the whole silicon chip and is not channeled as electric current in wires. The thermal sub-network must thus be refined, especially around the components which dissipate a significant amount of heat. The way the thermal mesh is built in our simulator and the way both thermal and electro-thermal sub-networks are linked are explained in [12,13].

3. High-level electro-thermal behavioral model

3.1. High-level behavioral modeling

The concept of electro-thermal high-level behavioral model has to be accurately defined with respect to the well known concept of the high-level electrical model.

A high-level electrical model is a set of analytical equations describing the behavior of a bloc, for instance an operational amplifier, which can be seen by the user as a black box with some input and output terminals. Let us consider the example of an operational amplifier. One of the behavioral equations could give the output voltage as a function of the input differential voltage ϵ, which is

$$V_{\mathrm{Out}} = f(\epsilon - V_{\mathrm{off}}) \tag{1}$$

where $f(\epsilon)$ is a non-linear function describing the non-linear output characteristic of the amplifier and V_{off} is its offset. The $f(\epsilon)$ function depends on parameters, at least on A_0, the open loop gain of the amplifier, and on the output saturation voltages $V_{\mathrm{Out}-}$ and $V_{\mathrm{Out}+}$. In a conventional high-level behavioral model, the parameters A_0, $V_{\mathrm{Out}-}$, $V_{\mathrm{Out}+}$ and V_{off} are given by the user. Let us now focus on V_{off}. Its value is ideally zero. Nevertheless, it is well known that the offset of an amplifier is highly sensitive to temperature, especially when a thermal gradient is present on the chip and that both input transistors of the amplifier input differential stage are not placed on the same isothermal. It is thus expected that an electro-thermal high-level model of this amplifier has to model such a thermal dependence of the offset. In addition, the thermal map of the chip depends not only on the heat generated by the cell to be modeled, here the operational amplifier, but also on the heat generated by the other cells of the chip, i.e. the cells surrounding the operational amplifier. This simple example shows that (i) the electro-thermal model of a bloc will depend on the layout of the bloc and (ii) the electro-thermal simulation of a chip cannot be done by parts since the electro-thermal behavior of the IC depends on all the elements in the chip, as well as on its package and ambient environment. These two points are very important. First, it means that an electro-thermal high-level model will be always associated to a physically designed bloc (hard IP – Intellectual Property). Second, it implies that the way the thermal dependencies of the model parameters are described has to take the possible heterogeneous thermal distribution over the considered IP. From all these remarks, the question is now how to build an IP electro-thermal high-level model? The first natural way to do it would be (i) to provide the black box, seen as a 3D black box, with some thermal ports, and to link these ports with thermal resistances and capacitances, (ii) to use the conventional electrical high-level behavioral model and to find a way to extract the dependence of the behavioral model parameters (A_0, V_{off},…) on the temperature of the thermal ports, i.e. to find a way to model the thermal dependencies of the behavioral model parameters on the possible no homogeneous thermal distribution above the IP. Nevertheless, as discussed in Section 2, by using such a method, the thermal sub-network would be too coarse and would result in very inaccurate electro-thermal simulations. As a consequence, on our point of view, a high-level electro-thermal model relies on (i) black boxes with one