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Temperature dependent timing in standard cell designs

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ABSTRACT

This paper proposes a methodology to simulate temperature dependent timing in standard cell designs. Temperature dependent timing characteristics are derived from standard delay format (SDF) files that are created by synthesis tools automatically based on SPICE characterizations. In addition, a fast calculation of temperatures using the equivalent Foster RC network is presented. A case study is also presented in this paper where the temperature dependent frequency variation of a ring oscillator is simulated demonstrating the necessity of temperature dependent timing simulations. An adaptively refineable partitioning method for simulating standard cell designs logi-thermally is proposed as well. This paper also introduces recent enhancements in the CellTherm logi-thermal simulator developed in the Department of Electron Devices, BME, Hungary. Finally, the simulation results are compared and verified with the SPICE compatible ELDO analog simulator from Mentor Graphics.

1. Introduction and motivation

In today's digital integrated circuits dealing with heating issues became a primary concern. As technology nodes and minimum feature size (MFS) keep shrinking device parameters tend to become more sensitive to process variations, supply voltage fluctuations and device temperature, to mention a few. These phenomena inferred the need for a simulation tool which is aware of process, temperature and supply voltage variations and can detect issues caused by such effects. A simulation framework is therefore needed to detect such problems and to allow for taking actions during the design phase, far before manufacture.

In this paper we demonstrate a methodology to constantly monitor device temperature during logic simulation and change cell propagation delays according to the current device temperature. This way we can predict operation of the circuit in a real environment encumbered with self- and ambient heating. Standard cell propagation delays are characterized by SPICE simulations and synthesis tools derive actual delay-temperature functions from cell placement and routing. The resulting sampled delay-temperature functions are stored in a Standard Delay Format (SDF) file.

The paper also shows a fast methodology to calculate cell temperatures using the analogy between the electrical and thermal domain. The methodology shows an easily implementable algorithm that calculates device temperatures using dissipated powers and the equivalent thermal Foster RC network of the structure.

2. Related work

In [1] Pable et al. deal with ultra-low-power signaling challenges caused by process, voltage and temperature (PVT) variations. Exponential dependency of subthreshold drive current on V_{th} and temperature in subthreshold operating region makes process and temperature variations of great interest while designing robust ULP systems. Small variation in the device V_{th} will translate into exponential variation in bias current and hence the device delay and power dissipation. The subthreshold phenomena addressed in the paper are potential sources of failures in a digital circuit. These issues must be addressed by a suitable simulator. Small changes in device V_{th} due to temperature variations can lead to timing problems that must be prepared for.

Rebaud et al. in [2] describe a new monitoring system, allowing failure anticipation in real-time, looking at the timing slack of a pre-defined set of observable flip-flops. They propose adaptive voltage scaling (AVS) and adaptive body biasing (ABB) to compensate PVT variations. Authors of [2] implemented a monitoring system on silicon to measure and adaptively compensate process variations. The dedicated sensor structures allow for real-time compensation of the mentioned effects. With a PVT variation-aware simulator engine the need for these extra sensor, monitor and compensation circuits might be eliminated as construction could be done in a PVT variation-aware manner.

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Lin et al. in [3] introduce a novel 9 transistor SRAM cell where PVT variations are taken into account. The proposed CMOS SRAM cell is PVT tolerant. The authors simulated their proposed 9 transistor SRAM cell with HSPICE and demonstrated excellent process variation tolerance. The PVT tolerance in this circuit is achieved by exploiting circuit techniques.

Kumar and Kursun in [4] attract attention to the fact that temperature-dependent propagation delay characteristics of CMOS integrated circuits will experience a complete reversal in the near future. They demonstrate that the speed of circuits in a 45-nm CMOS technology is enhanced when the temperature is increased at the nominal supply voltage. This is a quite interesting phenomenon contrary to the older technology generations. The inversion of delay-temperature functions in standard cell designs is a very important effect when simulating circuits with temperature-aware logic simulators. The reverse temperature effect described in [4] can be taken into account with the simulator proposed in this paper.

Authors of [5] introduce a sensor circuit with an area of 985 NAND2 equivalent gates that is capable of detecting whether a system is operating in the normal dependence or the reverse dependence region. This area overhead can be very significant especially for smaller designs. Digital standard cell circuits susceptible to temperature variations might be simulated with temperature-aware logic simulators and therefore such extra sensor circuits might be spared or their complexity might be decreased.

In [6] Sánchez-Azqueta et al. introduce a CMOS ring VCO design where PVT variations were taken into account. To overcome the limitation of the PVT variations, a tuning range of about 20% is sufficient for their ring VCO. The VCO mentioned in [6] contains a 4-stage ring oscillator. Compensating for process, temperature and voltage changes is also a main concern in VCO design and the presented demonstration circuit in this paper also utilizes a ring oscillator circuit to demonstrate frequency shifts caused by self-heating.

In [7] the leakage current, active power and delay characterizations of the dynamic dual V_t CMOS circuits in the presence of process, voltage, and temperature (PVT) fluctuations are analyzed based on multiple parameter Monte Carlo method.

In [8] Winther et al. show that using wirelength as the evaluation metric for floorplanning does not always produce a floorplan with the shortest delay. They propose a temperature dependent wire delay estimation method for thermal aware floorplanning algorithms, which takes into account the thermal effect on wire delay.

Golda and Kos [9] present the temperature influence on energy consumption and propagation time delay in CMOS ASIC circuits with several measurements.

Reviewing the present literature it turns out that there is a need for a simulator that can take process, voltage and temperature variations into account and especially self-heating of circuits during operation. This paper introduces such a simulator tool called CellTherm developed in the Department of Electron Devices, BUTE, Hungary.

In this paper the most recent improvements of the CellTherm [10,11] simulator engine are introduced. The CellTherm logi-thermal simulator is capable of simulating standard cell integrated circuit designs given with Verilog structural description. The simulator couples a standard compliant logic simulator (e.g. QuestaSim©, Incisive©) and thermal solver engine and calculates device temperatures in function of simulation time. CellTherm also reads the full layout, power and timing data of the design and calculates temperature-dependent delays of the consisting standard cells. This way CellTherm not only can detect hot-spots in the design but can back-annotate device timing and propagation delays during the simulation. CellTherm also can create heating animations of the design and watch out for thermally induced timing violations with the help of the logic simulator.

3. Design for demonstration

Our case study was a 0.516 mm × 0.353 mm standard cell digital circuit with four buffer cells driven with a 4-bit digital counter stimuli and a ring oscillator circuit. The process node was TSMC 0.35 µm. The design has been created from a synthesized Verilog description. For automated placement and routing Pyxis was used from Mentor Graphics©. This design was created in order to demonstrate the effect of temperature variations and evolving hot-spots on cell propagation delay. Cell delays and power dissipations have been extracted from the preceding SPICE simulations of the circuit.

Standard Delay Format (SDF) files were created from the extracted delay data for the temperature dependent timing simulation. To be able to visibly demonstrate the effect of temperature variation on delays, the propagation delay data in the SDF have been slightly modified manually. In spite of this, the true temperature dependence of cell delays has been simulated with SPICE.

In Fig. 1 the schematic layout of the design is shown. The P&R algorithm placed the cells in two rows. The four buffer cells were driven by an external stimulus like a 4-bit counter. The period of the counter was 1 µs. This feature has been implemented to demonstrate both self-heating and induced heating of the ring oscillator inverter chain. The inverter chain consists of 10 inverters and one kick-in NAND gate.

4. Grid partitioning

In CellTherm the surface of the standard cell IC can be divided into subregions called *partitions* where dissipated powers are accumulated and temperatures are calculated. The partitioning approach speeds up simulation times and initial database parsing in large designs containing more than 1000 standard cells. This approach makes the initial thermal model generation practically insensitive to the number of standard cells. Of course logic simulation can take longer for designs containing high number of cells, the time taken by the thermal engine to solve equations remains the same because thermal equations are generated for the partitioning grid not the standard cells.

Powers dissipated in partitions and temperatures of cell instances are calculated using the partition area and overlapping cell area ratio. This means that if a standard cell falls partly into a partition, then the cell's power dissipation is taken into account proportionally to the overlap ratio.

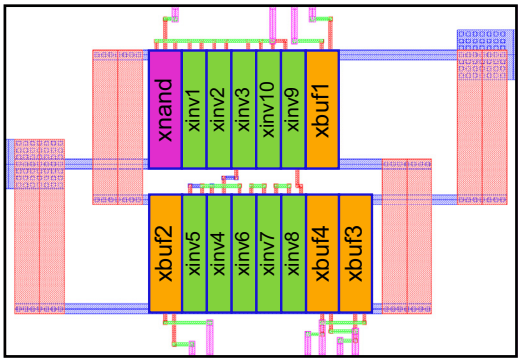

Fig. 1. Design layout of the ring oscillator circuit.