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Invited Paper

Fabrication of vertical thin-GaN light-emitting diode by low-temperature Cu/Sn/Ag wafer bonding

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ABSTRACT

Vertical thin-GaN LED was successfully fabricated on the GaN LED epi-layers grown on the patterned-sapphire substrate with the pyramidal pattern by low-temperature Cu/Sn/Ag wafer bonding at 150 °C. An inverted pyramidal pattern formed on the n-GaN surface after the GaN epi-layer was transferred onto Si wafer, which resulted from the pyramidal pattern on the patterned-sapphire substrate. The inverted pyramidal pattern has an equivalent function with roughening the n-GaN surface. With higher inverted pyramidal pattern coverage, the light extraction efficiency can be greatly enhanced. In addition, we found that the 4-fold increase (from 13.6% to 53.8%) in the pyramidal pattern coverage on patterned-sapphire substrate only gives the GaN LED epi-layer about 5.7% enhancement in the internal quantum efficiency.

1. Introduction

Recently, a new LED structure (vertical-GaN LED) was developed for the high-power LED applications [1–4]. The two key processes of vertical-GaN LEDs are (1) wafer bonding and (2) laser-lift off (LLO) techniques. First, the GaN/sapphire wafer has to be bonded with the transferring Si wafer. Then, the sapphire wafer was stripped off by KrF excimer laser (248 nm). Finally, the initial GaN LED epi-layers were transferred onto the Si wafer. So far, vertical thin-GaN LED are fabricated by using the GaN LED epi-layer grown on the planer sapphire substrate. The flat n-GaN/sapphire interface seems having better process window for focusing the laser beam during the laser lift-off process. Recently, the patterned-sapphire substrate techniques have been widely used in GaN-based LEDs [5,6]. With the break-through of the patterned-sapphire substrate technique, the efficacy of high-brightness GaN-based LEDs has been driven to a record-high of 150 lm/W [7,8]. The efficacy enhancement of GaN-based LEDs with the patterned-sapphire substrate technique is generally attributed to the improvement in both light extraction efficiency and internal quantum efficiency [9–13]. The regular patterns created on the sapphire substrate, which counteracts the effect of the total internal reflection (TIR) at the GaN/sapphire interface [9]. And, the enhancement in the internal quantum efficiency benefits from the reduction of threading dislocations by possible lateral growth of GaN epi-layer on the patterned-sapphire substrate [9,14–17].

Owing to the advantages of the patterned-sapphire substrate mentioned above, it would be of interest to fabricate the vertical thin-GaN LED chips with the GaN LED epi-layers grown on the patterned-sapphire substrate. For fabricating the vertical thin-GaN LED, the GaN LED epi-layers wafer first has to be bonded with a transferring substrate wafer by wafer bonding. Then, the patterned-sapphire substrate wafer would be stripped off. As a result, the GaN LED epi-layers can be transferred onto the desired transferring substrate, such as, Si wafer. How do the vertical thin-GaN LED fabrication processes affect the merits of the GaN LED epi-layers on the patterned-sapphire substrate has not yet been studied. For example, after the patterned-sapphire substrate being stripped off, the n-GaN layer with the inverted pattern would become the emitting surface. So, how does the inverted pattern on the n-GaN surface affect the light extraction efficiency (η_{LEE}), is an important issue to be understood. In this study, we fabricate the vertical thin-GaN LED chips with the GaN LED epi-layers grown on the patterned-sapphire substrate and study the effect of the inverted pattern on the performance of the vertical thin-GaN LED.

2. Experimental procedures

Numerous patterning features produced on the patterned-sapphire substrate by either dry etching or wet etching processes, which includes circle cavities, square cavities, hemispheric bumps and trenched stripes, have been studied [1,9,18–20]. Yet, no matter what etching process is used to create the patterns, a hard-mask (SiO_2 in most cases) lithographic process is required on the flat c-plane sapphire wafer. In this study, a mask-free wet-etching process was used to produce a so-called nature-patterned-sapphire substrate (n-pss). The n-pss wafers was done by immersing planar sapphire wafers into a mixing solution (H_3PO_4:H_2SO_4 = 3:1) at 260 °C for 30 min, and 60 min. Fig. 1 shows the SEM image of the

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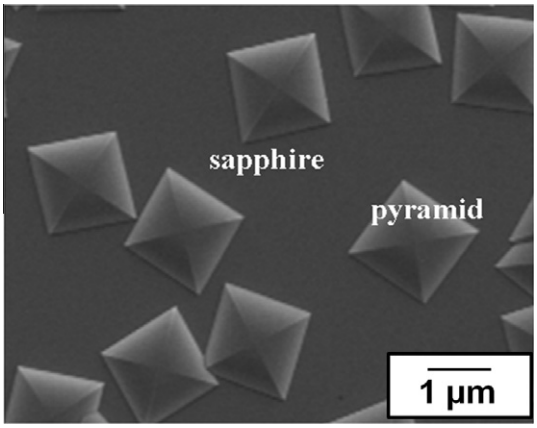

Fig. 1. SEM image of the pyramidal pattern on the etched sapphire wafer.

facet pyramids on the etched sapphire surface. The height and the width of the pyramid is about 0.2 μm and 1–2 μm, respectively. Then, GaN LED epi-layers were grown on the n-pss wafer with the pyramidal pattern by MOCVD process. The LED epi-layer structure includes a 1.8 μm thick undoped GaN layer and a 2.5 μm thick Si-doped n-type GaN cladding layer, an active region of 450 nm emitting wavelength with six periods of InGaN/GaN multiple quantum wells (MQWs), and a 0.3 μm thick Mg-doped p-type GaN cladding layer. After MOCVD epitaxial process, the GaN epitaxial n-pss wafers are ready for the fabrication processes of the vertical thin-GaN LED chips.

For fabricating the vertical-GaN LED structure, an excellent reflective metal layer is essential for the p-contact scheme on the p-GaN layer. Ag is known to have a high reflectivity in the visible regime. Prior to the deposition of the Ag reflective layer, a 20 Å Ni adhesion layer has to be deposited on the p-GaN surface. Then, a 2-μm Ag reflective layer are deposited on the p-GaN surface of the GaN epitaxial/sapphire wafers. Beside the function of the reflective layer the thick 2-μm Ag layer also serves as the bonding layer on the GaN/sapphire wafer side.

For the wafer bonding process, the Cu/Sn/Ag bonding system was studied in this present work. On the GaN/sapphire wafer side, 2-μm Ag layer is deposited as the bonding layer to bond with the Si wafer. On the Si wafer side, Cu/Sn bonding metallizations are prepared. The Cu/Sn metallization on the Si wafers were sequentially deposited with a 500-Å Cr adhesion layer, a 500-Å Pt barrier layer, a 500-nm Cu layer, and a 2-μm Sn bonding layer. The above metallization structures were deposited by E-Gun deposition process. The wafer bonding process is described below. First, the Si wafer and GaN/sapphire sapphire wafer with proper bonding metallizations were loaded into a graphite bonding fixture. Both wafers were intimately contacting with a compressive pressure of 2 MPa. Then, the sapphire/Si wafer bonding pair is placed in a vacuum furnace with a base pressure of 5×10^{-2} torr at 150 °C for 30–60 min.

After the GaN/sapphire wafer is bonded with the Si wafer, the back-side of the sapphire wafer was irradiated by KrF 248 nm excimer laser. A thin GaN buffer-layer right above the sapphire substrate absorbs the energy of the incident eximer laser and decomposed to Ga droplets and N_2 gas. As a result, the GaN epi-layer can be striped-off from the initial grown sapphire wafer. The by-product of the Ga metal droplets resided on the n-GaN surface, which would affect the subsequent analysis on the transferred GaN epi-layer. The dilute HCl acid solution (10%) was used to remove Ga droplets on the n-GaN surface. Then, the suitable n-contact metal Cr/Pt/Au pad can be fabricated on the cleaned n-GaN epi-layer. Fig. 2 illustrates the finished structure of a vertical thin-GaN LED chip on the Si substrate. The chip size is about 1 mm × 1 mm. After the process of n-contact pad, the finished LED chips were measured by an integral sphere measurement system.

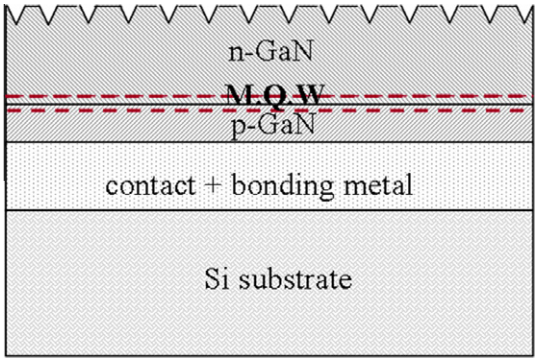

Fig. 2. The finished structure of a vertical thin-GaN LED chip on the Si substrate.

3. Results and discussions

Fig. 3 shows the SEM cross-sectional images on the bonding interface at 150 °C for 30–60 min. The SEM examination result

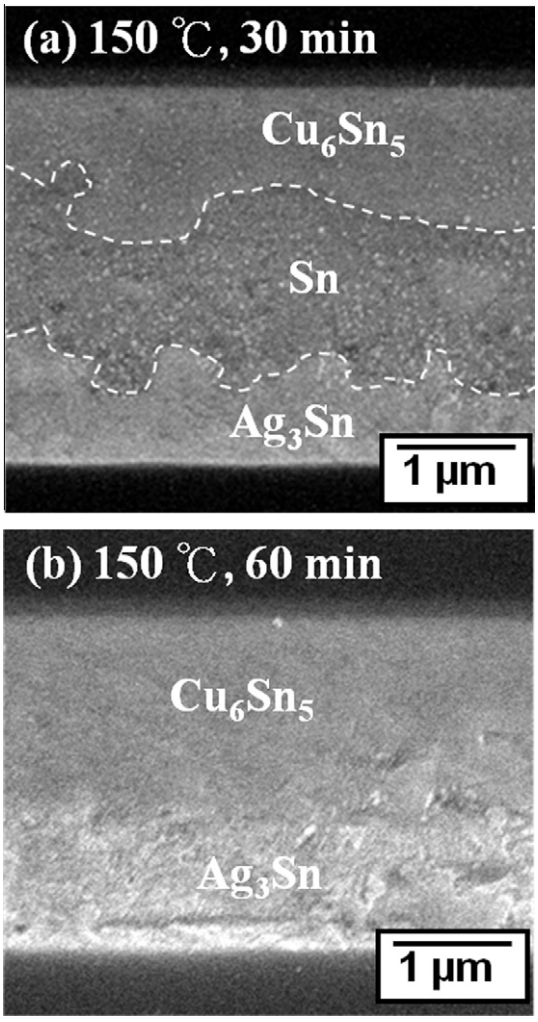

Fig. 3. The SEM cross-sectional images on the bonding interface at 150 °C for (a) 30 and (b) 60 min.