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A technique to mitigate impact of process, voltage and temperature variations on design metrics of SRAM Cell

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ABSTRACT

This paper presents a technique for designing a variability aware SRAM cell. The architecture of the proposed cell is similar to the standard 6T SRAM cell with the exception that the access pass gates are replaced with full transmission gates. The paper studies the impact of V_t (threshold voltage) variation on most of the design metrics of SRAM cell. The proposed design achieves 1.4× narrower spread in I_{READ} at the expense 1.2× lower I_{READ} at nominal V_{DD}. It offers 1.3× improvements in T_{RA} (read access time) distribution at the expense of 1.2× penalty in read delay. The proposed bitcell offers 1.1× tighter spread in T_{WA} (write access time) incurring 1.3× longer write delay. It shows 180 mV of SNM (static noise margin) and is equally stable in hold mode. It offers 1.3× higher RSNM (100 mV) compared to 6T (75 mV). It exhibits improved SINM (static current noise margin) distribution at the expense of 1.6× lower WTI (write trip current). It offers 1.05× narrower spread in standby power. Thus, comparative analysis based on Monte Carlo simulation exhibits that the proposed design is capable of mitigating impact of V_t variation to a large extent.

1. Introduction

Due to severe increase in V_t (threshold voltage) fluctuation caused by global and local process variations in ultrashort-channel devices, 6T SRAM cell and its variants cannot be operated at further scaled supply voltages without parametric and functional failure causing yield loss. Single-ended 6T SRAM cell [1] suffers from write delay. Low power 6T SRAM cell [2] could reduce access delay and write power but could not improve stability. None of the previous works has investigated the improvement of variability in SRAM cell at the circuit level in deep submicron. Therefore, robust and variation tolerant SRAM cell design technique capable of absorbing V_t shift due to RDF (random dopant fluctuation), and variation in other device and process parameters (such as length, width, oxide thickness, sub-wavelength-lithography, etching, and annealing) and still be able to perform expected functions need to be investigated. Trade-off must generally be made in terms of area to achieve this goal. To solve the read/write stability problems in the face of severe V_t variation in ultrashort-channel devices at aggressively scaled technology node such as 16 nm, this paper proposes a transmission gate (TG)-based 8T SRAM cell (hereafter called TG8T) and compares its performance with standard 6T SRAM cell at iso-device area. To verify the proposed technique, extensive simulations on HSPICE using 16 nm Predictive Technology Model (PTM) [3] are carried out.

The rest of the paper is organized as follows. Section 2 presents the proposed design and its read/write current analysis. Simulation results are discussed and compared in Section 3. Finally, the concluding remarks are provided in Section 4.

2. Proposed transmission gate based 8T SRAM cell

This section describes device sizing strategy and read/write current analysis of the proposed design.

2.1. Device sizing of proposed design

The primary motivation behind aggressive device scaling is to achieve improved performance and increased integration. These improvements come at the cost of increased sensitivity to PVT (process, voltage and temperature) variations and standby leakage, particularly in area-constrained circuit such as SRAM that employs minimum-geometry devices. An attempt is made in this work to mitigate these problems in traditional 6T SRAM cell by incurring minimum area penalty and retaining its fully differential architecture. This paper proposes a TG-based fully differential 8T SRAM bitcell (Fig. 1). And its design metrics are assessed and compared with its differential counterpart standard 6T (Fig. 2). As RDF induced V_t shift exhibits an inverse dependence on square root of device area (and is given by $\sigma_{vt} \propto EOT/\sqrt{(W \times L)}$, where

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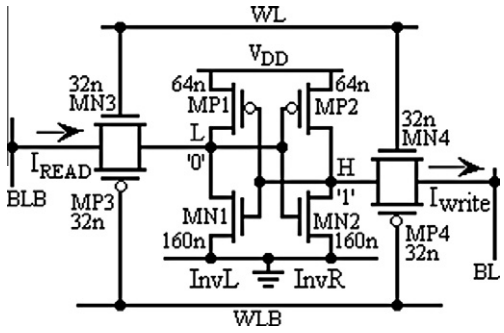

Fig. 1. Proposed TG-based fully differential 8T SRAM cell (TG8T).

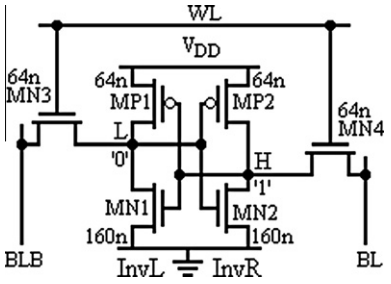

Fig. 2. Fully differential standard 6-transistor SRAM cell (6T).

EOT is effective oxide thickness, W and L are effective channel width and length), it appears that the simplest solution to the variability problem is to use larger device area. Hence, the design metrics of TG8T are compared with those of 6T with equal device area to demonstrate that the proposed design offers tighter spread in its parameters even at iso-device-area.

The use of increased device sizes to fight RDF is a critical piece of our design strategy. Using Monte Carlo (MC) simulations, device widths are set (Figs. 1 and 2) to meet robustness requirement with all device lengths set to 16 nm. As can be observed, for fair comparison, both the designs are at iso-device-area and bitline capacitance does not increase in spite of additional pMOSFETs. However, the proposed cell will consume 20% more silicon area because of WLB (wordline bar) routing and two additional transistors. The column architecture of the proposed SRAM is shown in Fig. 3. TG8T utilizes differential operation and does not require much architectural changes except adding a pMOSFET in parallel with each access nMOSFET (MP3 and MP4), thereby making it an 8T SRAM cell. An additional control WLB is needed to switch the access pMOSFETs. The WLB and WL (wordline) are non-overlapping complementary signals. Therefore, while accessing the cell all access FETs are switched simultaneously on for reading or writing. During hold mode all access FETs remain off.

2.2. Current analysis of the proposed design

Cell current or read current (I_{READ}) can be expressed analytically by solving Kirchoff's current law at internal node "L" storing "0", where current flows out through MN1 and goes in through MN3, MP3 and MP1.

$$\begin{aligned} I_{READ} &= I_{MN3}(V_{GS} = V_{WL} - V_L, V_{DS} = V_{BLB} - V_L) + I_{MP3}(V_{GS} \\ &= V_{WLB} - V_{BLB}, V_{DS} = V_L - V_{BLB}) = I_{MN1}(V_{GS} = V_H, V_{DS} \\ &= V_L) + I_{MP1}(V_{GS} = V_H - V_{DD}, V_{DS} = V_L - V_{DD}). \end{aligned} \quad (1)$$

Since MP1 is cut off because of $V_{GS} = V_H - V_{DD} \approx 0$, I_{READ} is the sum of the currents I_{MN3} and I_{MP3} that passes through MN1 while discharging precharged BLB (bitline bar).

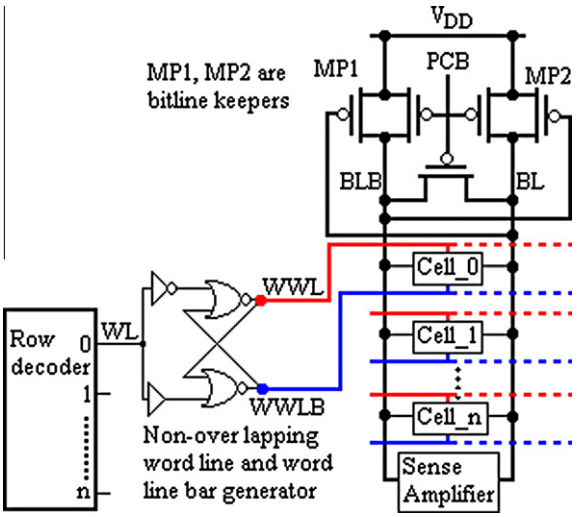

Fig. 3. Column architecture of proposed TG-based SRAM. Weak bitline keepers help in retaining bitline status at precharged value fighting against accumulated leakage current of unselected cells. Theoretical upper bound on number of cells sharing common bitline is leakage current of unselected cell and access time dependent.

The write-ability of a one half cell is determined by applying complementary signal to BL (bitline) and BLB. With BL = 0, I_{WRITE} is defined as a net current flowing out of internal node "H" storing "1"

$$\begin{aligned} I_{WRITE} &= I_{MP2}(V_{GS} = V_L - V_{DD}, V_{DS} = V_H - V_{DD}) - I_{MN4}(V_{GS} \\ &= V_{WL}, V_{DS} = V_H) - I_{MP4}(V_{GS} = V_{WLB} - V_H, V_{DS} \\ &= V_H) - I_{MN2}(V_{GS} = V_L, V_{DS} = V_H). \end{aligned} \quad (2)$$

Since V_L is usually small, the last term of I_{WRITE} is neglected. Thus I_{WRITE} is the current difference between pull-up device resisting the write and access devices discharging the node "H". Plots of currents against internal node voltage to obtain characteristic *N*-curve is shown in the following section.

The variation of currents results in the fluctuation in design metrics such as SINM (static current noise margin) and WTI (write trip current). With the assumption that, L, W, tox, and V_t follow independent Gaussian distribution, the variance of SINM and WTI can be obtained from simulation data [3],

$$\begin{aligned} \sigma^2_{SINM} &= \sum_i \left(\frac{\partial SINM}{\partial Li}\right)^2 \sigma^2_{Li} + \sum_i \left(\frac{\partial SINM}{\partial Wi}\right)^2 \sigma^2_{Wi} \\ &+ \sum_i \left(\frac{\partial SINM}{\partial toxi}\right)^2 \sigma^2_{toxi} + \sum_i \left(\frac{\partial SINM}{\partial Vti}\right)^2 \sigma^2_{Vti} \end{aligned} \quad (3)$$

$$\begin{aligned} \sigma^2_{WTI} &= \sum_i \left(\frac{\partial WTI}{\partial Li}\right)^2 \sigma^2_{Li} + \sum_i \left(\frac{\partial WTI}{\partial Wi}\right)^2 \sigma^2_{Wi} \\ &+ \sum_i \left(\frac{\partial WTI}{\partial toxi}\right)^2 \sigma^2_{toxi} + \sum_i \left(\frac{\partial WTI}{\partial Vti}\right)^2 \sigma^2_{Vti} \end{aligned} \quad (4)$$

where σL, σW, σtox, σV_t are the standard deviation (std. dev.) of device length, width, oxide thickness and V_t. The subscript '*i*' is the device number in the cell.

Read metrics such as read delay and I_{READ} are estimated with the development of 50 mV differential between BL and BLB. For this cell design, the operating mode, gate drives (V_{GS}), drain to source drives (V_{DS}) are reported in Table 1.