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Efficient design of parity preserving logic in quantum-dot cellular automata targeting enhanced scalability in testing

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ABSTRACT

Design of parity preserving logic based on emerging nanotechnology is very limited due to present technological limitation in tackling its high error rate. In this work, Quantum-dot cellular automata (QCA), a potential alternative to CMOS, is investigated for designing easily testable logic circuit. A novel self-testable logic structure referred to as the testable-QCA (**t-QCA**), using parity preserving logic, is proposed. Design flexibility of t-QCA then evaluated through synthesis of standard functions. The programmability feature of t-QCA is utilized to implement an ALU, realizing six important functions. Although the parity preservation property of t-QCA enables concurrent detection of permanent as well as the transient faults, an augmented test logic circuit (TC) using QCA primitives has been introduced to cover the cell defects in nanotechnology. Experimental results establish the efficiency of the proposed design that outperforms the existing technologies in terms of design cost and test overhead. The achievement of 100% stuck-at fault coverage and the 100% fault coverage for single missing/additional cell defects in QCA layout of the t-QCA gate, address the reliability issues of QCA nano-circuit design.

1. Introduction

CMOS technology is reaching its limit beyond which further downscaling in feature size is impossible. High leakage current, high power density levels and high lithography cost crop up with further dimension scaling. One of the emerging nanotechnologies, the Quantum-dot Cellular Automata (QCA), is considered as a viable alternative to meet the energy efficient design target beyond the limit of existing CMOS technology [1,2]. The major advantages such as low power consumption, zero power dissipation in signal propagation, high speed and high compaction density of QCA based design have attracted researchers to investigate its visibility and implementation constraints.

In VLSI circuits, parity checking techniques reduce the complexity of testing. The parity preserving logic gate, for which the parity of outputs matches with that of the inputs, when used with an arbitrary synthesis strategy for logic circuits, ensures detection of a fault at the primary outputs [3]. The testability feature provided by the existing parity preserving designs often takes the center stage, and the logical depth of a gate is ignored. Further, for testing such logic gate, an additional test logic circuit is considered without utilizing self testable feature.

In QCA paradigm, wire-crossings are a major overhead [4,5]. Gates that are highly programmable ensure that the larger circuits can be synthesized with fewer number of gates, and thus also reduce the number of wire-crossings. Since majority gate (QCA primitive) itself is not functionally complete, various QCA logic gates such as majority with inverter (MI), CMVMIN (coupled majority minority) [6], UQCLG (universal QCA) [7], NNI (nand-nor-inverter) [8], and AOI (and-or-inverter) [9] are conventionally used for realizing different QCA designs. The design and the fault tolerant capability of CMVMIN gate, reported in [10,11], are found to be acceptable. However, these gates do not have inherent fault detection or testing features.

All these above factors motivate us to design a new logic gate that can find a trade off between the QCA design costs for test logic and programmability of primary outputs. Also, to continue with the present days' VLSI progress, we move forward for emerging nanotechnology which is desirable to overcome the challenges of feature size reduction and reliability. The major contribution of this work, around parity preserving QCA architecture, can be summarized as follows:

(i) This work introduces a design methodology/framework in Quantum-dot cellular automata based on parity preserving logic. A new universal testable QCA logic gate termed as testable-QCA (t-QCA) is proposed. It is a 3×3 gate that realizes minority (min), majority (maj) and XNOR logic at its three primary outputs.

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(ii) The flexibility of this multi-purpose logic gate enables synthesis of different logic circuits such as benchmark functions as well as arithmetic logic unit. Experimental results establish the effectiveness of the proposed logic and it outperforms the existing technologies in terms of design cost as well as testing overhead.
(iii) Reliability issue in nano-circuit, the utmost necessity to overcome the high error rate, is addressed with the achievement of 100% fault coverage.
(iv) The parity preserving property enables a t-QCA for concurrent detection of permanent and transient faults by comparing the parity of its inputs and outputs. A simple augmented testing circuit is also proposed, using QCA primitives, that functions as the cost effective comparator.
(v) Finally, the flexibility and testability of parity preserving logic are revisited for nano-circuits.

The paper is organized as follows. Section 2 deals with the basics of QCA. Section 3 provides related work on parity preserving circuits. Section 4 introduces the proposed design and evaluates the performance of t-QCA. High level logic synthesis with t-QCA is reported in Section 5. Test evaluation of the t-QCA, subjected to all possible defects, is summarized in Section 6. Section 7 concludes the paper.

2. Preliminaries

In QCA based design, a single device (QCA-cell) is used for construction of all the components of a circuit (computational elements and wires). The schematic diagram of a four-dot QCA cell is shown in Fig. 1(a). It contains four quantum dots positioned at the corners of a square and two free electron [2]. A quantum dot is a region where an electron is quantum-mechanically confined (Fig. 1(a)). The coulombic repulsion causes the classical model of electrons to occupy only the four corners of QCA cell, resulting either polarization $P=-1$ (logic 0) or in $P=+1$ (logic 1) as shown in Fig. 1(b).

The basic structure realized in QCA is the 3-input majority gate, $MV(A, B, C)=Maj(A, B, C)=AB + BC + CA$ (Fig. 1(c)). The majority gate can also function as a 2-input AND or a 2-input OR by fixing one of the three input cells to $P=-1$ or $P=+1$ respectively.

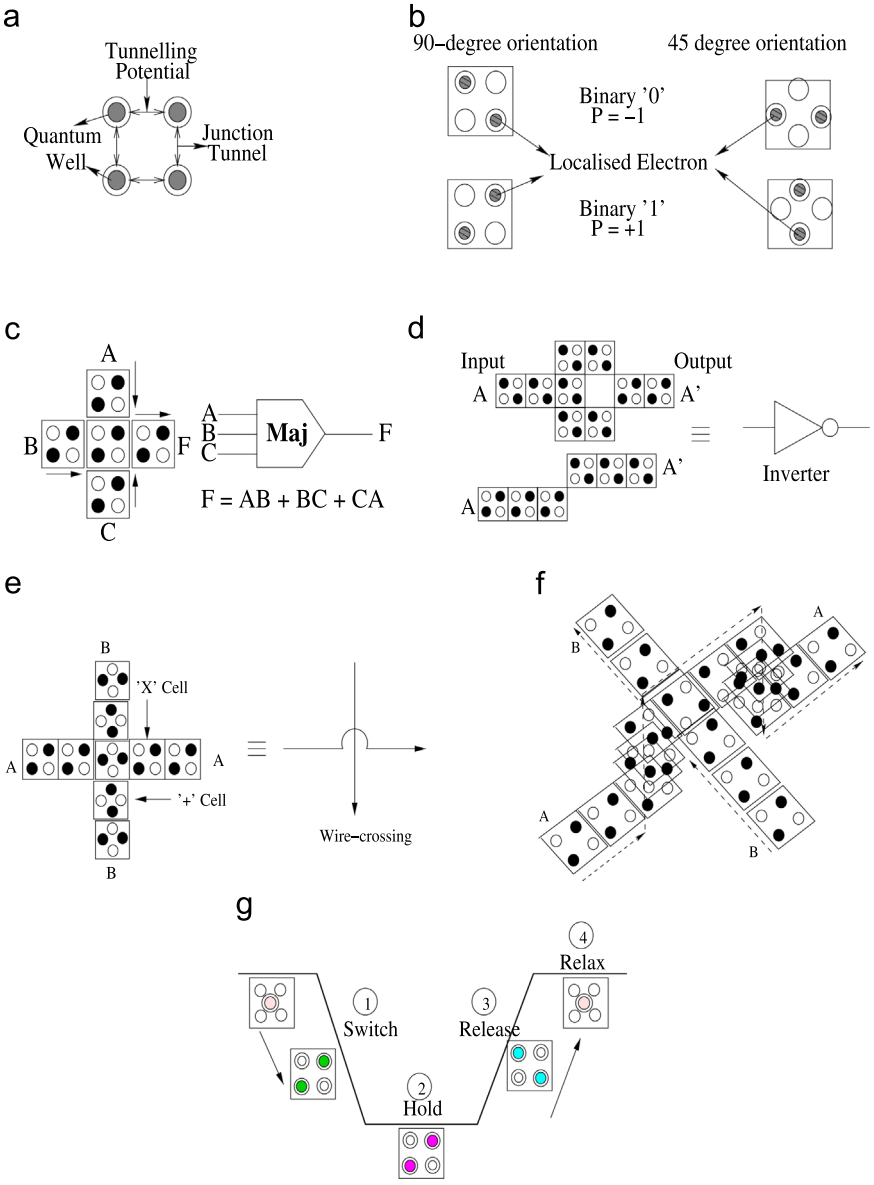

Fig. 1. (a) QCA cell, (b) QCA cell with two different polarizations, (c) majority voter, (d) inverter, (e) co-planar wire-crossing, (f) multilayer wire-crossing and (g) clocking.