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A low-power low-offset dynamic comparator for analog to digital converters

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ABSTRACT

A comparator comprises a cross coupled circuit which produces a positive feedback. In conventional comparators, the mismatch between the cross coupled circuits determines the trade-off between the speed, offset and the power consumption of the comparator. A new low-offset low-power dynamic comparator for analog-to-digital converters is introduced. The comparator benefits from two stages and two operational phases to reduce the offset voltage caused by the mismatch effect inside the positive feedback circuit. Rigorous statistical analysis yields the input referred offset voltage and the delay of the comparator based on the circuit random parameters. The derivations are verified with exhaustive Monte-Carlo simulations at various corner cases of the process. A comparison between typical comparator and the proposed comparator in 180 nm and 90 nm has been made. The power consumption of the proposed comparator is about 44% of the conventional and its offset voltage is at least one-third of other mentioned conventional comparators.

1. Introduction

The growth in portable battery operated communication devices increases the demand for low power and high speed ADC. Generally, moving toward the smaller feature size allows for the reduction in the power consumption and higher speed. However, the process variation and mismatch increases at finer processes and limits the performance of the ADCs. One of the critical parts of an ADC greatly influenced by the process variation and mismatch is the comparator [1]. In some ADCs, the offset voltage can be tolerated to some extent, thanks to the digital error correction (DEC) and over-range protection [2,3]. However, the INL and DNL characteristics of the ADC are still influenced by the comparators offset even in the DEC enabled ADCs.

The characteristics of a comparator are defined by its input referred offset voltage for a given power dissipation, speed and the area [2]. Scaling CMOS technology shrinks the headroom voltage and the full scale range of input voltage. Therefore, the protection range of the offset voltage decreases. Moreover, CMOS device mismatch nearly doubles for every process generation below 100 nm. This effect gives a major thrust in recent comparator designs [4]. Hence, the design of a high performance comparator is one of the key challenges in an ADC design.

In comparators, a lower offset comes at the expense of larger transistors hence higher power consumption and reduction in speed. In addition, the conventional comparators are complex to design and there are only few design methodologies to control the offset. To reduce the power consumption and the area of comparators, dynamic comparators are proposed [5]. However, such comparators usually suffer from relatively large offset voltage than static comparators [6,7]. Some architectures have been proposed for dynamic comparators in the literatures. The dynamic comparators are categorized into three groups: Resistor divider [5], Differential pair and Capacitive–differential pair dynamic comparator [2]. Other structures are mainly derived from these architectures [8–12].

A typical single phase comparator is shown in Fig. 1 that was introduced in [5] to show the trade-offs between the offset and the speed and power. The structure is called “Lewis–Gray” comparator, and is widely used in ADC architectures [9]. Hence, it is taken as the reference conventional comparator in this paper. The core of this comparator is the same among all single phase comparators comprising a preamplifier stage and a cross couple latch. The two stages operate asynchronously and simultaneously when the comparator enters the evaluation phase. Therefore, in the ideal case where the cross-coupled latch does not have a mismatch, it operates only when the preamplifier induced a sufficiently large differential voltage at the internal nodes of the latch. Practically, the offset due to the mismatch of the cross-coupled latch kicks in as soon as the entire amplifier begins to operate.

Recently, an analysis was made to estimate the input referred offset voltage of the conventional comparator [13]. It was shown

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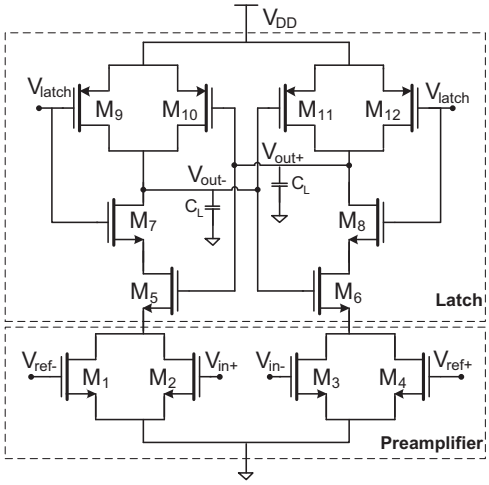

Fig. 1. Conventional fully differential dynamic comparator [5].

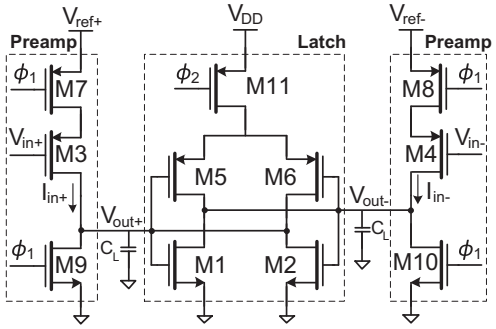

Fig. 2. Proposed comparator.

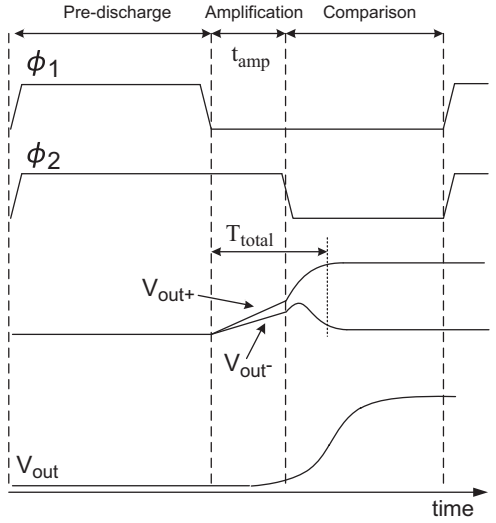

Fig. 3. Conceptual waveforms.

how the comparator input referred offset can be reduced at the expense of a high power dissipation. That is because, at the comparison phase the regeneration process in the cross coupled pairs and the amplification of the input voltage occur simultaneously. Hence, the amplification by the input transistors must be fast and large enough to fight against the offset of the cross coupled pairs. A large and fast amplification leads to a higher power consumption. It was concluded that the mismatch between M_7 and M_8 alone can lead to 0.3 V offset voltage in 45 nm technology [13]. Moreover, the comparator itself has high sensitivity to the output capacitor mismatch [9]. The positive feedback at the output increases the effect of the capacitor mismatch on the overall input referred offset which again demands a more powerful input stage.

In order to break the deadlock between the offset and the power consumption, a new architecture is proposed. The double phase architecture takes the advantage of a cascade of amplifying stage and a usual latch stage. More importantly, it involves a significantly smaller input offset voltage without a significant power and area penalty. The rest of this paper is organized as follows: In Section 2 the new comparator architecture is presented along with the analysis of its offset voltage. In Section 3 the simulation results are presented while Section 4 concludes the paper.

2. Proposed comparator

2.1. Circuit architecture

The proposed comparator is shown in Fig. 2. The latch circuit is separated from the amplification branches. Each stage operates independently with different clock pulses, ϕ_1 and ϕ_2. This separation helps the input transistors to overcome the mismatch effect inside the latch circuit before the offset of the latch circuitry is involved in the overall decision making process. Hence, it significantly reduces the input referred offset voltage of the comparator. Moreover, the comparison of the differential input voltage with the differential reference voltage takes effect at the gate source of the input transistors, M_3 and M_4, leading to fewer transistor count regarding to conventional architecture and therefore lesser offset from mismatch between these transistors.

The proposed comparator works with a special three phase signaling. The signal waveform of the comparator is illustrated in Fig. 3. At the first phase or pre-charging phase both ϕ_1 and ϕ_2 are high. Therefore, the cross coupled inverter pairs are off and pre-charge transistors discharge the output nodes to the ground. The second phase or the amplification phase will occur when ϕ_1 is low and ϕ_2 is still high. Consequently, the path to the ground is cut while the reference voltages can feed the input branch and let the input cascade transistors conduct. The difference between the amount of the current produced in the input branches, $I_{in+}-I_{in-}$, is related to the voltage difference between the input and the reference differential voltage. During the amplification phase, the currents set the differential voltage at the internal nodes of the cross-couple latch, V_{out+} and V_{out-}. In the third phase, the comparison phase, the latch circuit operates and the induced differential voltage is boosted in the regenerative loop of the cross-coupled inverters.

2.2. Analysis

2.2.1. Decision point

A simple analysis shows that the comparator compares the voltage difference between the input differential voltage with the reference differential voltage, $V_{REFDIFF}$. At the beginning of the amplification phase, the output nodes are discharged to the ground ($V_{out+}=0, V_{out-}=0$).

The amplification phase starts with the activation of ϕ_1. Transistors M_8 and M_7 operate as a small resistor at the source of the input transistors M_3 and M_4. Since, the voltage level at the inputs of the comparator at the decision point is more than zero, the drain–source voltage of the input transistors is more than their gate–source voltage. Hence, M_3 and M_4 operate in saturation