Microelectronics Journal 44 (2013) 706–711

Contents lists available at SciVerse ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Reconfigurable gate array architecture for logic functions in tunneling transistor technology

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ARTICLE INFO

Article history:
Received 4 August 2012
Received in revised form
19 November 2012
Accepted 13 May 2013
Available online 4 June 2013

Keywords:
Single-electron transistor (SET)
Reconfigurable SET logic
Circuit simulation

ABSTRACT

This work describes the design of a reconfigurable logic gate array composed of single-electron tunneling (SET) transistors currently under investigation as potential *post-CMOS* candidates for future nano-scale integrated circuits for use in low-power embedded systems. A layer in the proposed array consists of a SET summing-inverter block replicated in subsequent blocks and extended to implement flexible logic functions in terms of the sum-of-products (SoP) and products-of-sum (PoS) forms. The reconfiguring of the array can be accomplished through the alteration of a block's logic function by way of a control voltage. The reconfigurable array can work normally at room temperature and can flexibly realize functions with better performance at lower power compared with pure MOSFET circuits.

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1. Introduction

The continued growth and advancement of the semiconductor industry has been driven by the exponential increase in the density of solid-state integrated circuits (ICs) due to reduction of the feature size of the conventional MOS silicon transistor. Smaller dimensions have permitted a remarkable improvement in the overall circuit performance and an equally considerable cost cut-back of the fabricated components. Nonetheless, as the transistor feature size enters the nanometer-scale regime, its behavior becomes increasingly problematic as new physical phenomena at short dimensions occur and limitations in material properties are reached [1]. The main challenge is then to develop pioneering technologies that will extend the scaling beyond roadmap projection. Several nanoscale device replacements for bulk-effect semiconductor transistor have been suggested [2,3] to circumvent the CMOS scaling problem. These devices can take advantage of the quantum mechanical effects such as tunneling and energy quantization, which occur naturally in the nanoscale regime. An example of such a device is the single-electron tunneling device first proposed by Averin and Likharev [4] suitable for implementing ultra dense and ultra low-power architectures [5] and potentially high-speed logic [6]. Moreover, recent advances in silicon based fabrication technology [7] show the possibility for room temperature operation. Similar to other future technology candidates, SET devices display a periodic switching behavior that differs from traditional MOS devices giving rise to new paradigms in logic design and processing. Some of these examples include SET/CMOS hybrid multivalue logic [8], multiband filtering circuits [9], and analog pattern matching circuits [9].

Recently, the area of reconfigurable logic has been the focus of investigation by various groups [10,11]. In our previous work [12], we introduced the concept of programmable logic constructed with *summing-node* SET inverter blocks. In this paper, we extend our previous work to design a reconfigurable logic array (RLA), which consists of fully connected four layers that generate logic functions synthesized in SoP *minterms* and PoS *maxterms* forms. We first present simulation results and stability diagrams and then discuss the performance of the logic array in terms of power dissipation, propagation delay, and gain. We also offer insight on the direction of this research in the area of hybridization of CMOS and SET, which can be applied to the logic array. The graphs presented in this paper were generated using a Monte Carlo tool [13] demonstrating the correct and stable operation of the reconfigurable SET logic gates and array. The stationary or non-transient simulations were used to calculate the operating points, assumed to be the equilibrium points, which are essentially snap-shots of some solution trajectory. The transient simulations were used to examine the propagation delay in the SET logic circuits. The remaining part of this paper is structured as follows. Section 2 discusses reconfigurable SET logic and shows simulation results and Section 3 presents performance analysis of the logic array. Section 4 concludes the whole paper.

2. Reconfigurable SET logic

As previously mentioned, SETs are candidates for post-CMOS era due to their appealing features that include scalability as well as the low-power property if the issues of background charge and

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http://dx.doi.org/10.1016/j.mejo.2013.05.002

device-to-device variations can be solved [1]. In addition, since SET transistors exhibit a periodic switching behavior, they can be fitting for designing reconfigurable logic gates. The building block of our configurable array is the summing node-inverter that consists of multiple voltage signals V_1, $V_2 \ldots V_n$ with capacitive inputs, C_1, $C_2 \ldots C_n$ coupled to a summing node of the SET inverter as shown in Fig. 1. The SET arrangement can take advantage of the adjustment of Coulomb oscillation phase to realize reconfigurable logic, which cannot be done with MOSFETs. If we consider three input voltages V_1, V_2, and V_3 as the digital signals A, B, and C shown in Fig. 2(a), the output is a NAND function when a fourth input V_4, referred to as the *select* input to the summing node, is set to low or 0 V. Conversely, when the *select* is set to high or 0.5 V, the output is a NOR function as shown in Fig. 2(b).

Since SETs inherently have low gain, the output voltage swing can be slightly increased by applying a small negative voltage ~0.05 V in place of the ground connection. Ultimately, MOS sense amplifiers in a SET/CMOS hybrid configuration become a requisite to amplify the output voltage of the SETs to match the logic levels. The simulation conditions at 300 K were $C_j = 0.1 \times 10^{-19}$ F, $R_j = 0.1$ MΩ, $C_g = 1.5 \times 10^{-19}$ F, $C_{in} = 2 \times 10^{-18}$ F, $C_L = 3 \times 10^{-19}$ F, and 0.55 V as the drain-source bias.

Our proposed SET array has two reconfigurable NAND planes followed by a SET adder [14] that implements the XOR function, shown in Fig. 3. The first level in the RLA layered structure, shown in Fig. 4, passes the input signals or generates their complements using inverters while the second NAND plane evaluates the product terms. The third NAND plane combines the product terms to generate the minimized SOP of an arbitrary function $F = \Sigma(1,2,3,5) = X'Y + Y'Z$ and the last XOR level produces the original function when XORed with 0 and the complemented function when XORed with a high input.

In Fig. 5(a) and (b), the NAND product terms are obtained by setting V_3 in the summing-inverter SET circuit contained in layer 2 and 3 of Fig. 4 array to a low.

The third plane generates the NAND of the product terms $[(X'Y)'(Y'Z)']'$ that can be simplified to the SOP form $(X'Y) + (Y'Z)$ by DeMorgan's law. The output waveforms for that plane are shown in Fig. 5(c). In the 4th plane of the SET NAND RLA, the output of the XOR can give the function $[(X'Y) + (Y'Z)] \oplus 0 = (X'Y) + (Y'Z)$ or its complement $[(X'Y) + (Y'Z)] \oplus 1 = [(X'Y) + (Y'Z)]'$ as displayed in Fig. 5(d).

Our SET RLA can be reconfigured to implement the same function in POS by setting V_3 in the summing-inverter SET circuit contained in layer 2 and 3 of the array in Fig. 6(a) to a high, which alters the NAND to a NOR function by adjusting Coulomb oscillation phase.

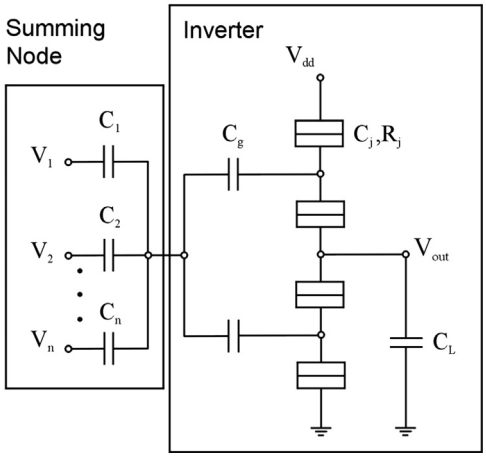

Fig. 1. Schematics of a summing-inverter SET circuit.

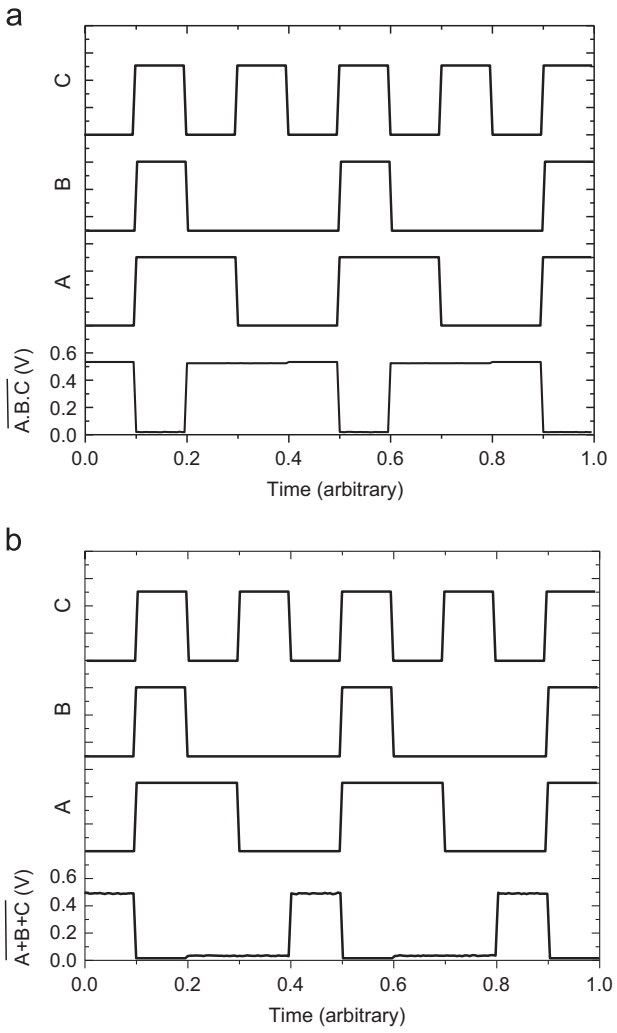

Fig. 2. (a) SET NAND output waveform and (b) SET NOR output waveform.

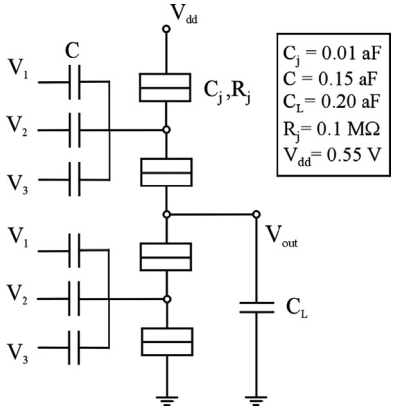

Fig. 3. Schematics of a SET XOR.

The simulation results of the minimized function $\Pi(0,4,6,7) = (X'+Y')(Y+Z)$ are shown in Fig. 6(b). As can be observed from Figs. 5(d) and 6(b), the output waveforms are matching, i.e. $\Pi(0,4,6,7) = \Sigma(1,2,3,5)$ since minterms and maxterms have complementary-symmetry relationship as expressed by DeMorgan's laws.

With the purpose of checking the stability and the steady operation of the SET reconfigurable logic gates and array at room temperature, we obtained the stability plot provided by the Monte Carlo simulator. This plot is a grayscale diagram where the white

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