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Single-ended, robust 8T SRAM cell for low-voltage operation

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ABSTRACT

Recently, an SRAM has been in the development stage, with its objective to withstand the ever-increasing process variations as well as to support ultra-low power applications, even at subthreshold supply voltages. In this paper, a new 8T SRAM cell, which employs a single bitline scheme to perform the write and read operations, is proposed. This scheme enhances the write ability and read stability by cutting off the feedback loop of the inverter pair, thereby eliminating the read and write constraints on the transistor dimensions. Additionally, it efficiently trims down the write power and standby power consumption. The experimental results show that the proposed 8T cell achieves 4.66× write ability, 2.33× read noise margin, 28.0% write power reduction, and 3.3× lower standby power dissipation when compared with a 6T bit-cell at 0.5 V through a Monte Carlo simulation (10,000 times) using the TSMC 65-nm process. Moreover, it also achieves higher process variation tolerance at an ultralow operating voltage.

1. Introduction

SRAMs always occupy most of the area and dominate the main performance and power in VLSI systems. Continuous downscaling of the process technology has led to an increased integration density and improved device performance; however, it has also led to increased power consumption, particularly the consumption of leakage power. Some of the battery-operated devices such as cell phones, medical instruments, and wireless body sensing networks have stringent power constraints. Lowering the supply voltage is one of the most straightforward and effective ways to suppress energy consumption because reducing the supply voltage could reduce the dynamic power quadratically and leakage power remarkably. Although operating voltage reduction along with device scaling has brought many benefits, it has also created some serious problems such as stability and reliability challenges.

With the miniaturization of devices, intradie process variations including random dopant fluctuation (RDF) and line edge roughness (LER), increasing leakage current, and decreasing Ion-Ioff ratio have become serious issues, which have resulted in a significant loss in the operating stability. This limits the circuit operations to a large extent, particularly in the ultra-low voltage regions. SRAMs are more sensitive to the preceding described cases than the logic circuits, owing to the minimum or sub-ground-rule-size transistors in the cell. The degraded stability of the SRAM cells is further exacerbated by the scaled voltage. This can result in various memory failures including read, write, hold, and access time failures [1]. In addition, the memory failure probability will highly increase in the future process nodes [2]. Therefore, the data stability of the SRAM cells becomes a top priority in low-operating voltage environments.

The standard 6T SRAM cell, as shown in Fig. 1, fails to perform reliably at a low voltage because of the intrinsic read disturbance produced by the voltage division between the access transistors and the pull-down transistors. Furthermore, there are strict constraints on the size of the access transistors and pull-up transistors to support the data stability and functionality of the write operation. For improving the write margin and read stability of the conventional 6T SRAM cell, various read and write assist methods have been explored, including the virtual cell-ground [3–5], adaptive cell-VDD [6–10], dual-rail supply power [10–16], dynamic boosted or reduced wordline voltage [10,11], [17], negative bitline voltage [15,18–21], and write-back schemes [22–24]. However, the minimum operating voltage (V_{min}) in these schemes has been limited owing to the collision requirements of the read stability and write ability, and the best performance is achieved only at a V_{min} of 0.45 V. This has become a bottleneck for 6T SRAM cells to be applied at a lower voltage.

Also several new 5T–10T SRAM cells have been proposed [25–51] for low-voltage applications. These bit cells shown in [25–39] achieve excellent read stability by isolating the read path from the storage nodes. However, all these cells employ the same complementary bitline pair for data transfer as standard 6T cells and cause a large area overhead. The write scheme still has a write operation constraint on the transistor dimensions and consumes a significant amount of the write switching power owing to the

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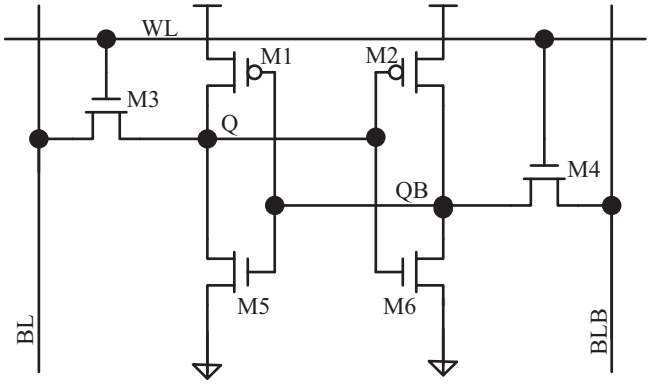

Fig. 1. Standard 6T SRAM cell.

heavy capacitance loading on the bitlines. In addition, single-ended (SE) bit cells used in [40–51] can effectively reduce the active and leakage power of the bitlines; however, these cells require additional control circuits and compensation schemes to maintain their write ability and read stability. In other words, these bit cells are still restricted by the read or write constraints.

In this paper, a novel SE and robust 8T SRAM cell is proposed for low-voltage applications. The cell performs write or read operations through only one bitline, thereby decreasing the leakage and active power consumption. Moreover, the proposed 8T cell increases the write and read margins by cutting off the positive feedback loop of the inverter pair, thus completely eliminating the write and read operation constraints on the transistor dimensions. The experimental results show that the proposed 8T SRAM cell exhibits a 4.66 × write margin and 2.33 × read margin improvement, when compared with the standard 6T cells, at a supply voltage of 0.5 V in a Monte Carlo (MC) simulation (10,000 times), as well as 28.0% write power reduction and 3.3 × lower standby power consumption. The remainder of this paper is organized as follows. The proposed SE 8T SRAM cell and the read/write operation schemes are described in Section 2. In Section 3, the simulation results and comparisons are elaborated. The final section presents the conclusions.

2. Proposed 8T SRAM cell

The conventional SE SRAM cells [35] have a severely degraded write "1" static noise margin (SNM) due to the threshold loss of the storage nodes and the voltage dividing effect between the access transistors and the pull-down transistors, particularly at a low supply voltage. An SE 7T SRAM cell [40] is proposed to alleviate the write "1" problem of the single bitline, as shown in Fig. 2 (a). It eliminates the SNM in the read operation because of the separate read port and uses the differential-VSSM biasing arrangement (VSSM1 and VSSM2) to improve the write ability. These VSSM lines are boosted (by V_{ss}+ß) differentially depending on the input data. However, the Diff-VSSM 7T SRAM cell needs additional control circuits and compensation schemes to maintain its write ability and reliability, which results in an array area overhead and a complex floor plan.

In the proposed SE 8T SRAM cell, as shown in Fig. 2(b), data storage is performed by an asymmetrical cross-coupled inverter pair, invL (the left inverter) and invR (the right inverter). Only one write bitline (WBL) and one read bitline (RBL) are used to perform the write and read operations, respectively. Two transistors (M3 and M5) embedded in the invL assist in the write and read operations.Wordline (WL) is enabled both in the write mode and in the read mode. The write wordline (WWL) is activated only in

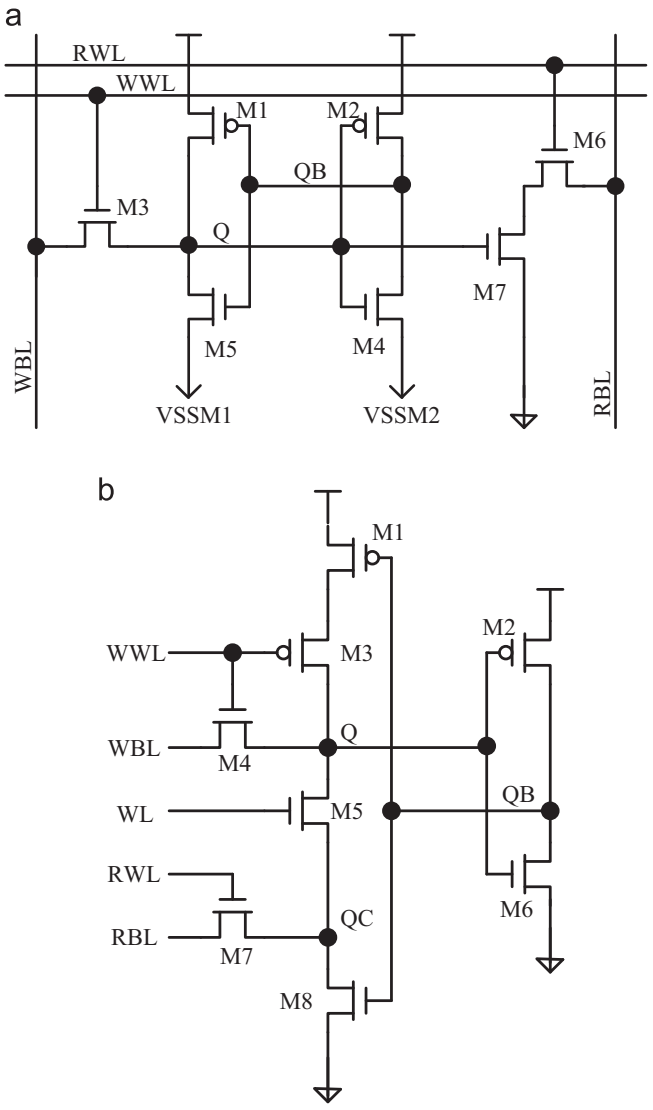

Fig. 2. Schematics of SRAM cells. (a) Diff-VSSM 7T cell. (b) The proposed single-ended 8T cell.

Table 1
True table of proposed 8T cell.

	Hold	Write-0	Write-1	Read
WWL/WBL	0/0	1/0	1/1	0/0
RWL/RBL	0/1	0/1	0/1	1/1
WL	1	0	0	0

the write mode, and the read operation is performed by enabling the read wordline (RWL) signal. Table 1 lists the truth table of the proposed 8T cell for different operational modes, and the corresponding signal waveforms of the write and read operations are described in Fig. 3.

2.1. Single bitline write scheme with loop-cutting

This scheme is used to reduce the write active power consumption and improve the write ability. When the cell is in the write "1" mode, the WWL is activated and the WL signal remains low. Further, M3 and M5 are turned off and the WBL is transferred through M4 to the storage node Q (Fig. 4). During the entire write