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New methodology for thermal analysis of multi-core processors based on dedicated ASIC

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ABSTRACT

Accurate prediction of thermal phenomena occurring in multi-core processors manufactured in new technologies prove to be both crucial and challenging. Therefore, in this paper, we introduce a new methodology for thermal analysis of such chips. The novelty of our approach is the use of a dedicated ASIC (*Application-Specific Integrated Circuit*), composed of a 16×24 array of heat cells, which emulates the power dissipation in a real processor and allows observing the chip temperature distribution in real-time. The ASIC takes as an input the power trace computed by the execution of benchmarks on a cycle-accurate processor simulator. The entire methodology flow is thoroughly described in the paper, including the details about the chip design and power modeling techniques. Post-layout simulations of our ASIC are used to verify the correctness of the design, whereas our approach to power modeling is validated using preliminary thermal simulations performed with existing software tools.

1. Introduction

Thermal analysis of integrated circuits is of enormous importance and will even be more crucial in near future. Temperature is a major source of malfunctions in integrated circuits. It has also been estimated that a 10 °C rise in the device temperature reduces its lifespan by the factor of two [1]. Moreover, for several years now the parameter which limits the operating frequency of processors is the maximal power density which may be dissipated in a given area. At the same time, growing demand on computational power and current trends in high-performance computing show that the number of cores integrated on a single processor die will continue to grow. Some authors expect processors with dozens or even hundreds of cores to be produced soon [2]. With technology scaling, as we approach feature sizes of several nanometers, new thermal phenomena are expected to occur in these VLSI (*Very Large Scale Integrated*) chips. In particular, the impact of thermal coupling grows with each technology node. Therefore, it becomes more and more difficult to accurately predict the thermal effects in multi-core processors using current tools, which often use simple thermal models to be able to provide the reasonable simulation time. On the other hand, the accurate simulation of a multi-core chip using FEM-based tools (*Finite Element Method*) would require a prohibitively long time. Therefore, the authors of the paper decided to elaborate a thermal processor simulator which will not suffer from the performance/accuracy tradeoff. Our approach allows the simulator to run a cycle-accurate execution of various applications and dynamically compute the transient temperatures in every part of the chip within reasonable time. The main novelty of the proposed approach is the use of a custom-designed dedicated ASIC, which serves a thermal emulator of a true multi-core processor.

The paper is organized as follows: the second section explains the proposed simulation methodology. The details about the chip design are presented in Section 3. Next section is devoted to the results of post-layout simulation of the designed ASIC with particular emphasis on the current DAC (*Digital-to-Analog Converter*). In Section 5 power modeling methodology is presented while Section 6 contains the preliminary thermal simulations performed with software thermal modeling tools. Last section concludes the paper.

2. Simulation methodology

The outline of the proposed thermal processor simulator is shown in Fig. 1. Power traces are computed using the standard approach known from many previous works [3]. In short, a cycle-accurate simulator like Simplescalar [4] executes a benchmark and an integrated power simulator (like for example Wattch [5]) is used to periodically evaluate the average power dissipated in every processor component in a given time period. However, unlike other works, in our approach this power trace is not used as an input to the software thermal simulator. Instead of

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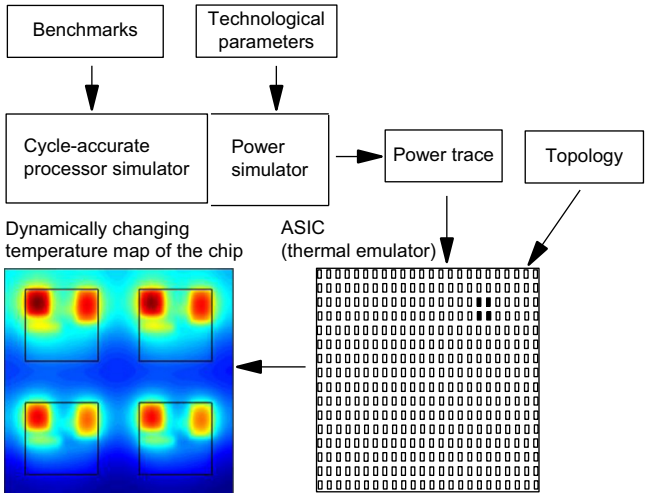

Fig. 1. Outline of thermal simulation methodology.

calculating temperatures using analytical models, we propose to obtain chip temperatures using a dedicated ASIC — a thermal emulator which "mimics" the power dissipated in components of a real processor. The thermal measurements of the ASIC will be done on-chip using integrated temperature sensors. Experiments will be performed on a special measurement stand consisting of the dedicated multichannel data acquisition card and the dual cold plate cooling assembly with Peltier thermo-electric modules allowing active control of cooling conditions [6].

The idea of our thermal ASIC is that the chip is mainly composed of a regular array of heat cells [7], in which the power dissipated in each cell can be independently controlled and changed at relatively high frequency. Each heat cell consists of two power MOS transistors whose current (and therefore power) can be digitally controlled (see Section 3 for details). Additionally, each heat cell incorporates a temperature sensor enabling temperature readout. Consequently, we obtain a very flexible chip architecture:

- to each heat cell, we can assign a specific power which will be dissipated in this area,
- very accurate thermal map of the entire chip can be obtained by periodically reading the temperatures of the temperature sensors, located in each heat cell,
- the power dissipated in the heat cells can be changed at relatively high frequency while observing the temperature in the chip.

This versatile structure allows thermal modeling of any multi-core architecture provided that the power dissipated in the chip elements is *a priori* known. In our approach, the power trace file is converted into input data sequence for the ASIC and thus used to generate a dynamic temperature map (see Fig. 1). Let us consider an example for clarity. Let the four black rectangles in Fig. 1 correspond to the ALU (*Arithmetic Logic Unit*) of one of the cores in a quad-core chip. Using the power simulator, we obtain the power dissipated in this ALU in a given time period, for example 1 W power dissipation during 100 ms is reported. Consequently, in our test chip we set the four heat cells to dissipate exactly 1 W during 100 ms. The same method is used for all processor blocks and for the entire simulation time. Simultaneously, the temperature data from our chip is read, which allows obtaining the dynamic thermal maps of the processor during the execution of the benchmark. Such thermal simulations can be repeated for different core configurations, technologies, cooling conditions or benchmarks. It will certainly allow investigating the potential occurrence of hotspots and help to investigate the problem of thermal coupling, which in our opinion will be especially important in the 16 nm technology and beyond. Such an approach can be also very helpful when evaluating the efficiency of various DTM (*Dynamic Thermal Management*) techniques.

3. ASIC design

This section presents details of the proposed ASIC architecture with special attention paid to the power cell which is the basic block of the proposed chip. It should be emphasized that the design of a real multi-core architecture is difficult and expensive to realize, thus the authors developed a test ASIC in an older technology, in which large heat sources represent particular functional processor blocks. In this way, it is possible to emulate the thermal behavior of state-of-the-art multicore processors based on the analysis of a chip manufactured in a much less expensive technology. After thorough analysis the authors decided to use the 0.35 μm CMOS high voltage technology provided by *austriamicrosystems*® (AMS).

The layout of the heat cell (see Fig. 3) needs to be considered carefully since the position and size of the high voltage transistors (heat sources) play an important role during thermal simulations. The distribution of hot spots constitutes an additional constraint which is usually not taken into account during the design of analog circuits.

The presented ASIC consists of 384 power (heat) cells which represent the power dissipation sources in real many-core processors. The total area of one heat cell is about 0.05 mm^2 and all cells form a 16×24 array. The main parts of the heat cell are the heat source and temperature sensors (see Figs. 2 and 3). The heat source is constituted by the output of a configurable current mirror – two power MOS transistors which can be seen in Fig. 2 – connected to high voltage source of 50 V. The current mirror output can sink up to 10 mA, which gives maximal power of 0.5 W per heat cell. It is assumed that power contribution of other transistors in the heat cell is negligible due to their relatively low supply voltage (3.3 V).

The actual current flowing through the power MOS transistors, and consequently the dissipated power, is set by a 3-bit DAC placed in every heat cell which scales reference external current using one of 8 levels according to actual configuration stored in a shift register added to each power cell. The DAC output current is than copied with ratio 4 to 1 into the power MOS transistors in order to achieve final value of dissipated power. Quality of current scaling and copying is crucial in order to obtain reliable heating conditions. Therefore the DAC and power transistors had to be carefully designed taking into account their electrical behavior as well as area constraints.

In general a DAC performance can be characterized by a set of parameters covering its static and dynamic behavior [8]. The authors found DC characteristics as the most important with regard to application with the proposed thermal simulator. Special attention was paid to linearity issue. The goal was also to minimize difference of the output current between different power cell with the same configuration taking into account gain and offset variations of the DC characteristic across the chip.

4. Post layout simulation

All simulations described in this paragraph were carried out in the Cadence® IC/Spectre and Matlab environments. The former tools were used to verify the ASIC design against electrical