Microelectronics Journal 44 (2013) 382–392

Contents lists available at SciVerse ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Behavioral model of folded and interpolated ADCs for test evaluation—Case study: Structural DfT method

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ARTICLE INFO

Article history:
Received 4 October 2012
Received in revised form
25 January 2013
Accepted 4 February 2013
Available online 16 March 2013

Keywords:
Folded and interpolated A/D converter
Behavioral modeling
Circuit simulation
Matlab environment
Mixed-signal testing

ABSTRACT

This paper presents a behavioral model for folded and interpolated analog-to-digital converters that takes into account non-idealities in the converter blocks. ADC performances are extracted by a Matlab/Simulink simulation to analyze how faults, considered as variations in the different parameters used for the description of each building block, affect the overall and local behaviors. This model also permits the evaluation of different test approaches (in an individual or comparative way). In this work we have developed a case study in which a structural Design-for-Test method has been preliminarily evaluated with good results. This methodology consists in sampling several internal points of the converter at the same time, so that, by computing relative variations among them, the presence of a defect can be detected.

1. Introduction

Nowadays, analog-to-digital converters are common blocks in mixed-signal circuits. In a particular case of embedded high-speed ADCs, they are used in a wide range of applications such as satellite receivers, new generation DVD players, interfaces with storage elements such as computer hard-disks, or the emerging ultra-wide band radio technology [1]. In order to be suitable for the demanding digital telecommunication market, these converters require, besides high speed, low linearity errors and low power consumption (battery-powered devices). In this sense, folded and interpolated ADCs [2–5] represent a suitable alternative to flash architectures when low-to-moderate resolution and low-power are required, due to their smaller number of comparators and chip area while almost maintaining the conversion speed of the flash type.

An ADC is a complex mixed-signal circuit in which thorough transistor-level simulation to explore design options or to evaluate calibration or test techniques is a time-consuming and, in many cases, almost unaffordable task. Consequently, it is advisable to carry out an analysis at a higher level of abstraction through behavioral models of the system for a preliminary evaluation, allowing the design and/or test engineers to estimate the effect of limitations of basic blocks on the overall performances at a lower cost.

As far as the state-of-the-art of behavioral models for ADCs is concerned, in the last years we can highlight their usefulness for the evaluation of synthesis tools and several top-down design methodologies for discrete and continuous-time sigma–delta converters [6–8], pipeline architectures [9,10], reconfigurable interpolated flash ADCs [11], or time-interleaved topologies [12]. These high-level models can also constitute a desirable tool to assess the validity of calibration or post-correction schemes in the particular cases of sigma–delta [13], pipeline [14], full-flash [15] or time-interleaved converters [16].

Traditionally, ADCs are verified through a specification-based test that consists in a long sequence of parameter characterization through rather complex and quite demanding processing algorithms, in terms of accuracy, speed and data storage, to obtain the complete static and dynamic performance of the converter [17]. Consequently, the evaluation of any new test approach is another suitable issue for the application of behavioral analysis. In the literature we can find examples of this application: a mixed-signal test technique that utilizes sigma–delta modulators as test vehicles, together with correlation techniques [18]; or a behavioral-based method for test vector generation [19].

In the particular case of folded and interpolated ADCs, very few contributions can be found in the literature exploring their behavioral modeling, and always considered as tools to provide a set of design criteria satisfied by the different building-blocks that constitute the architecture [20]. There is a lack of models for testing purposes to characterize this ADC topology.

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0026-2692/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.mejo.2013.02.016

This work proposes a Matlab/Simulink [21,22] behavioral model of a folded and interpolated ADC not only to explore and verify how the limitations of the building-blocks affect the ADC performance from a functional point of view, but also to preliminarily assess a structural test approach that aims to reduce the inherent high test cost of functional testing by targeting the existence of defects rather than measuring electrical performance parameters. The aforementioned lack of previous works in this field highlights the novelty of this contribution.

Finally, a structural Design-for-Test strategy can further reduce the aforesaid test cost by considering the test needs of a system throughout the design process. In this sense, this work also presents a case study where a structural DfT method that monitors internal test points of the converter has been evaluated. The voltage deviation among these test points is the parameter chosen to infer the presence of a defect in the CUT.

The paper is organized as follows: Section 2 presents the basic structure of the folded analog-to-digital converter used. Section 3 describes the behavioral model of the ADC blocks and their circuit parameters. In Section 4 the ADC performances are extracted and analyzed to establish how faults affect them. Section 5 describes a case study in which the behavioral model is used for the evaluation of a structural DfT method. Finally, Section 6 states the conclusions.

2. Folded and interpolated A/D converter (FI ADC)

Despite their simple design and inherently good high-frequency behavior, the main disadvantage of full-flash ADCs is the significant number of comparators required (2^B-1, where B is the resolution of the converter), resulting in large chip area and power consumption. Moreover, these comparators should have a low input offset, thus demanding large transistors for matching reasons or the use of offset compensation techniques.

By introducing analog preprocessing in the form of a "*folding amplifier*" or "*folder*," the number of comparators and their requirements can be significantly reduced, since the analog folding architecture allows each comparator to detect more than one zero-crossing point. The number of zero crossings is referred to as the "*folding factor*", and it lessens the number of comparators by nearly the same factor [2].

A common folded and interpolated architecture divides the codification process into two steps performed in parallel: a coarse encoder for the most significant bits and a fine subsystem for the least significant bits [2–5]. The most popular method to generate folding signals utilizes coupled differential pairs [23] in the folder block (FB). Besides that, an interpolation network, usually made up of a string of equal resistors, can produce additional folding signals, allowing circuit complexity and power consumption to be further reduced. Furthermore, this interpolation network acts as a resistive averaging step that lowers the offset impact [24] within the comparators.

The folded and interpolated ADC chosen in this work (Fig. 1) uses a distributed implementation of a sample-and-hold (S&H) function. It has been reported that the use of a front-end S&H block can reduce the bandwidth constraint affecting the folder block and the interpolator due to the frequency multiplication effect [5]. Moreover, a distributed function in the input gain stages is much less demanding than a single sample-and-hold amplifier before the converter as the gain in the S&H stages helps to relax the offset requirements in the folding circuitry by a factor equal to this gain. Finally, this input stage makes synchronization between coarse and fine bits unnecessary.

The coarse analog preprocessing circuit of the ADC in Fig. 1 generates analog versions of the MSB bit, MSB-1 bit, and also signals to detect overflow and underflow conditions. The final output code is provided by a digital encoder circuit, which processes the outputs of the comparators detecting the zero-crossing of the differential outputs from the folder blocks and the coarse preprocessing module.

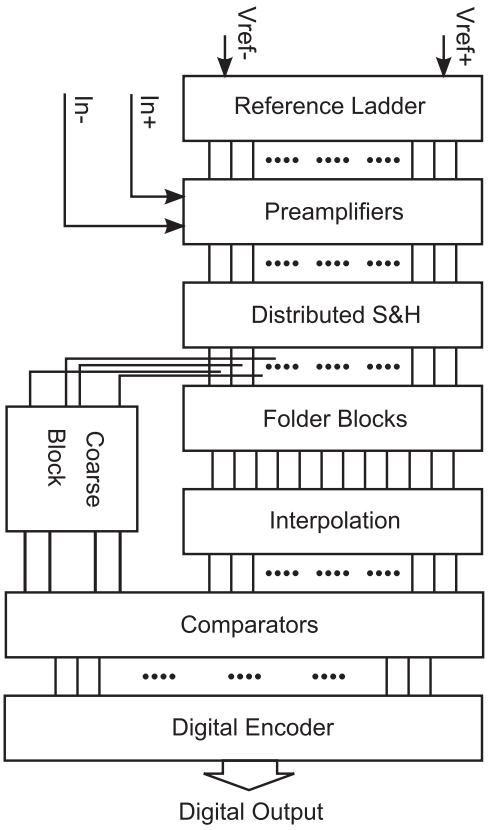

Fig. 1. Block diagram of the ADC.

3. Behavioral ADC model

The high-level Matlab/Simulink behavioral model designed for the FI ADC introduced in Section 2 has been developed to allow, not only the optimization of the ADC architecture, but also the evaluation of specification-based and structural test approaches, considering a number of second and upper order effects that, for accuracy reasons, should be taken into account.

Consequently, the aforementioned model must include block parameters that permit the extraction of the local and overall specifications of the ADC, both static and dynamic, in faulty and fault-free conditions. For example, a dynamic specification such as the signal-to-noise and distortion ratio (SINAD) is obtained by a Fast Fourier Transform (FFT) test of the ADC digital output code. In the same way, by means of a histogram test, the static parameters, such as the Differential and Integral Non-Linearity (DNL, INL), are calculated.

Moreover, the model must also enable the analysis of voltages and currents from each sampled block for the evaluation of a structural test method such as the case study presented here. Therefore, comparison of detection results is possible.

The main high level parameters used for modeling the different converter blocks implemented in the MATLAB/SIMULINK environment are as follows:

- Reference ladder and interpolation network: nominal resistance value and sigma variance.