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Application of time resolved emission techniques within the failure analysis flow

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Abstract

As the number of transistors and metal layers increases, traditional fault isolation techniques are less successful in exactly isolating the failing net or transistor to allow physical failure analysis. One tool to minimize the gap between global fault isolation – by means of emission microscopy or laser based techniques (TIVA, OBIRCH) – and physical root cause analysis is Time Resolved Emission (TRE). This paper presents two case studies illustrating the application of TRE within the failure analysis flow to generate a reasonable physical failure hypothesis.

1. Introduction

Fig. 1 illustrates a typical failure analysis flow. Due to the small feature size of new technologies, global fault isolation methods like emission microscopy or laser based techniques like TIVA and OBIRCH [1,2] cannot perform an exact failure localization to a single transistor because of limited spatial resolution.

In addition to this, in many cases these methods do not show the direct failure location, but only the effect of a failure like an emission spot on a floating node. A local fault localization method is needed. However, the spatial resolution of Time Resolved Emission is the same than the above mentioned global fault isolation methods. But with the knowledge of the transient behaviour of the probably failing nodes it is easier to generate a reliable failure hypothesis.

However, the increasing number of metal layers does in many cases no longer allow connecting the nets of interest via FIB-pads and micro probing.

This paper demonstrates the use of Time Resolved Emission (TRE) within the FA flow to generate a more reliable failure hypothesis and successful physical root cause visualization.

2. Principles of time resolved emission

Today, Light Emission is a popular effect studied in semiconductor devices. Time Resolved Emission allows a dynamic characterization of the DUT at the transistor node-level. This FA technique intends to stamp the timing of the transistor switching event in a known probing area. The infrared photo emission collected is the faint energy released by hot-carriers during saturation mode [3–5].

The equipment used for the next analysis is an Emiscope-III system from Credence. Fig. 2 details the contents of this system.

The photo-detector is an Avalanche Photo Diode [6]. This APD, if quenched, sends a signal to the pTA. picoseconds Timing Analyser – that bins the timing information into a histogram.

An ATE applies a stable pattern in continuous loop mode to the DUT as the system is able to collect one

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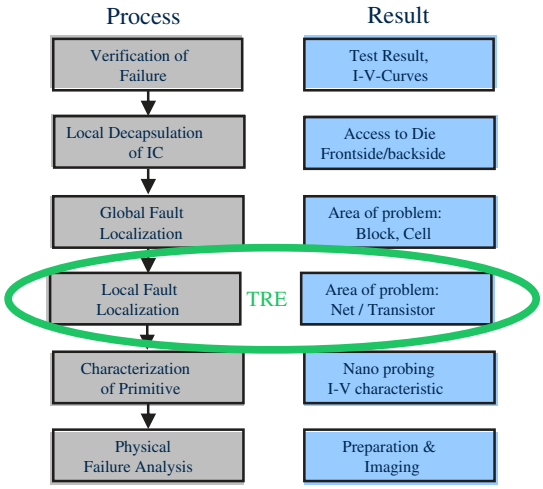

Fig. 1. Principal FA flow; application of TRE marked.

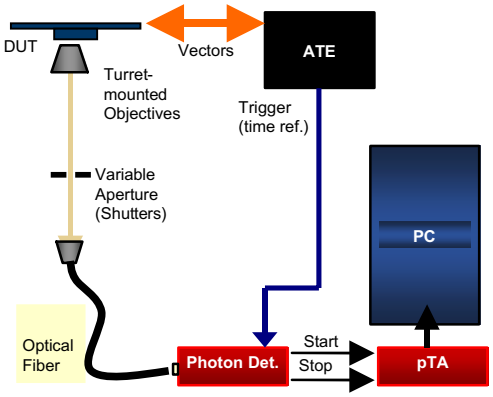

Fig. 2. EmiscopeIII and ATE block diagram in acquisition mode.

photon per loop. A trigger signal coming from the ATE is used as timing reference for all measurements.

Histogram curves show up different peaks that might correspond each to a switching event. These curves can be filtered or processed to extract useful signals more efficiently [7]. High-to-low emission that involves NMOS transistors is brighter than Low-to-high from PMOS transistors due to the slower hole mobility compared to electrons. In that way, the user is able to rebuild logical waveforms.

This method is purely non-invasive and is done through the DUT backside. The Solid Immersion Lens – thanks to its high magnification and NA – delivers the best collection efficiency to get the fastest relevant results by suppressing the air to silicon interface [8]. Typically, few seconds are enough to get results for 90 nm gate length devices operating around 1.2 V with the EmiscopeIII generation [9].

A direct CAD link helps to navigate quickly to the location to probe. Besides a layout overlay horizontal and vertical shutters allows the probing of the desired transistor only. Thus, the logical waveforms can be reconstructed at the transistor-level, or some other effects like static emission for known logical levels can be understood.

3. Case studies

The following case studies highlight the TRE usage in the FA flow to localize efficiently the fault at the transistor node-level and to continue successfully with physical analysis.

The device of the first case study was manufactured in a 130 nm copper technology with six metal layers. It failed due to a systematic scan failure detected by statistical scan analysis (SSTA) [10,11] at the fab.

The ATPG tool came up with a failure hypothesis on several nets causing a short. Fig. 3 shows a layout snapshot with highlighted fault candidates. The search area of 350 μm × 950 μm on five metal layers was too large for classical failure analysis (top down preparation and imaging). Therefore, global fault isolation by means of TIVA was performed (see Fig. 4) to allow concentrating on one of the failure hypotheses.

A weak TIVA signal was detected at buffer A. However the search area was still too large to start with physical

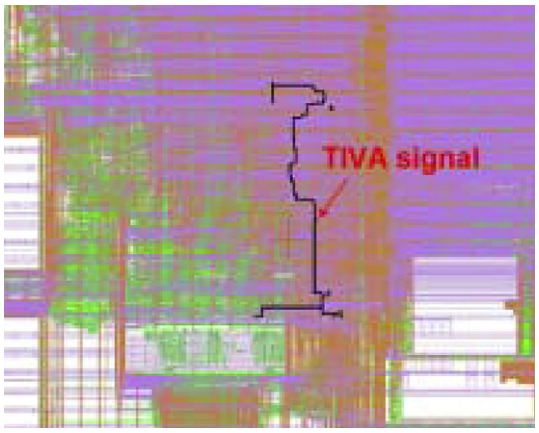

Fig. 3. Layout with highlighted fault candidates (black), location of TIVA spot marked.

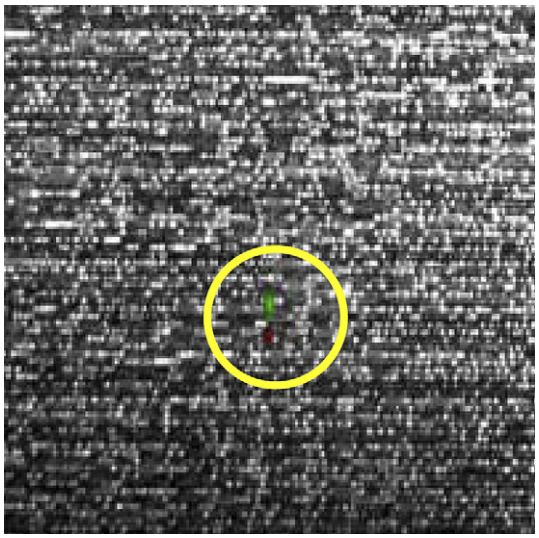

Fig. 4. Global fault localization; weak TIVA signal.