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NBTI product level reliability for a low-power SRAM technology

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Abstract

We present a methodology to investigate product level NBTI reliability for the 90 nm technology node including the correlation between transistor, circuit, and product level NBTI reliability. NBTI reliability lifetime, dielectric breakdown, and gate leakage currents pose an important limitation to the maximum applicable supply voltage across the gate oxide. Product standby currents and regulator design are highly influenced by transistor reliability. We will present product reliability data ensuring sufficient product level reliability as well as their correlation attempts to transistor level reliability data.

1. Introduction

The demand for ever higher drive currents and better performance has pushed the gate oxide thickness towards its material limits, especially as we enter the 65 nm and 45 nm technology nodes. The common candidate for the ultimate gate dielectric, silicon dioxide, is facing its structural boundaries and silicon dioxide/nitride stacks/compositions will become mainstream for 65 nm technologies and beyond. The medium dielectric *k*-number of nitride allows thicker physical oxides to control direct tunneling currents. However, the ultimate dielectrics are high *k*-number gate materials such as hafnium oxide or zirconium oxide. Both dielectric materials have demonstrated recently comparable carrier mobilities, but still suffer from dielectric integrity issues and reliability problems. Severe charge trapping effects reduce the reliability drastically and new breakdown phenomena never experienced before with silicon dioxide based gate oxides have been observed [1,2].

We will focus on nitrided gate oxides in this presentation and discuss the different reliability concerns. As drive currents increase HCI reliability usually gets worse since the drive current directly determines the carriers generated by impact ionization. Lightly-doped drain (LDD) optimization, however, reduces the electric field at the drain edge significantly. Overall the substrate current, which is a quantitative measure for impact ionization, is strongly reduced for advanced CMOS technologies.

The second considerable reliability concern is time dependent dielectric breakdown (TDDB). The TDDB lifetime is usually measured in the weak inversion regime. Generally, the lifetime is strongly dependent on the maximum junction temperature, the applied maximum gate voltage and the stressed gate oxide area. The maximum applied gate voltage in a circuit is mostly limited by the gate induced leakage current (GIDL) for low power products which can be the major off-state leakage current component. For high speed 90/65 nm technology products the maximum gate bias is chosen to meet the performance requirements. TDDB can be mostly improved by lowering the gate stress or by understanding the circuit behavior of the critical transistors in more detail. The TDDB lifetime significantly improves if AC signals are applied to the stressed transistor compared to a constant DC stress. Generally, TDDB lifetime improves for a higher nitrogen concentration in the gate oxide, but it also causes more positive charges being created during NBTI stressing [3]. The biggest concern with regards to TDDB reliability results from the recent trend of over driving the transistors with higher gate voltages to improve the saturation currents. The gate overdrive causes a significant impact on the gate oxide

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reliability and does not improve the fundamental CV/I performance metrics. This trend has been recognized in the recent ITRS roadmap, where the supply voltages have been adjusted to higher values reflecting the urge for higher drive currents [4]. Oghata et al. [5] have given the time to breakdown for different gate oxides over a wide range of stress voltages. A very consistent trend is found for the power law exponent for NMOS and PMOS transistors justifying the use of the power law voltage dependence to evaluate dielectric breakdown for ultrathin gate oxides (<35 A). Historically, the E-model or 1/E models were used to model the dielectric breakdown voltage dependence.

Contrary to HCI degradation TDDB shows a strong temperature dependence and degrades with elevated temperatures. Since the drive currents degrade at higher temperatures the hot carrier generation rate also degrades leading to higher HCI lifetimes. For TDDB the lifetime degrades significantly due to the increase of the bulk trap generation rates leading to percolation currents in the gate oxides [6]. For practical purposes the TDDB lifetime depends significantly on the detection of the onset of soft breakdown vs. hard breakdown. Different soft breakdown models have been discussed in the literature. However, engineering judgment is still used to determine the exact soft breakdown event.

2. NBTI reliability

Since the introduction of heavily nitrided gate oxides the NBTI phenomena gained significantly on importance. Significant work has been published on the NBTI reliability for standard DC test conditions ($V_s, V_d, V_b = 0.0$ V) as well as under pulsed conditions [7–10]. The relaxation phenomena was deeply investigated and characterized. We will present experimental data which clearly show the impact of the measurement equipment as well as relaxation time between stress cycles on the overall NBTI reliability. However, the role of hydrogen is still not fully understood [10]. Less work was published on the circuit level reliability degradation due to NBTI and the impact of relaxation. We analyze all possible circuit level biasing conditions, maximum operating temperatures, and operating cycles to understand the impact on the circuit level. A simple analytical reliability model is referenced to estimate the threshold voltage shift during real operation conditions. This additional threshold voltage shift is counting against the design margin budget and, hence, has to be added to the SS corner at elevated temperature in order to evaluate the worst case circuit conditions.

In the following sections we will focus on three levels of investigations: the transistor level, the ring oscillator level (RO), and the product level. It will be shown that each of this reliability levels will have significantly different results with respect to NBTI lifetimes demonstrating that NBTI is a very complex phenomena which might be very difficult to link from transistor level to product level. Historically that is a huge paradigm shift for reliability engineering since the other two reliability components (HCI and TDDB) can still be estimated on a product level by analyzing the transistor level data.

3. Transistor level reliability

Numerous transistor level reliability data and degradation curves have been published in the recent literature on NBTI. It can be noted that mostly saturation drive current, threshold voltage or linear current degradation is reported. Since those quantities are fundamentally connected they can be correlated easily. The degradation was measured using a probe station employing a S–M–S (stress/measure/stress) technique where the relaxation time was approximately 10 s between the stress and the measurement stage. Hence, significant relaxation occurred in the early switching cycles during the measurement stage which results in recapturing of some hydrogen at the interface to repair the broken interface bonds. Fig. 1 shows the same gate oxide measured in a package level testing system which has a relaxation between the stress and the measurement cycle of 700 ms compared to a bench system. It can be clearly shown that relaxation gives false readings in the early phases of the stress experiment for the bench measurement, whereas the degradation curves converge at higher stress levels suggesting that recovery is limited at longer stress intervals. The recovery phenomenon has been reported extensively in the literature and was attributed to the re-passivation of the broken Si–H bonds at the Si-gate oxide interface by hydrogen [11]. So far it is still not clearly understood what the detailed mechanisms are, however, the impact of relaxation can be easily validated by stressing a PMOS transistor and afterwards releasing the stress and measuring the recovery (see Fig. 2).

Almost 40% of the damage recovers after 30 min of relaxation. The level of recovery depends on the local stress equilibrium at the gate oxide and the availability of hydrogen to re-passivate the dangling Si bonds to form a Si–H bond again. A simple reaction–diffusion model is com-

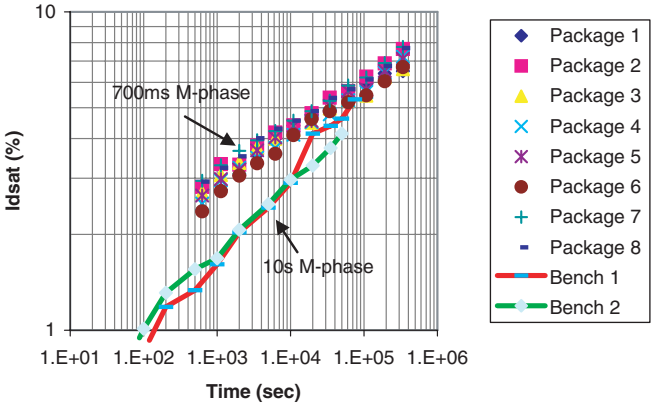

Fig. 1. NBTI Idsat degradation for different S–M–S methods. Package level (symbols) and bench (lines) testing show the impact of relaxation at the early stress phases due to the measurement equipment limitations.