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Through-silicon-via insertion for performance optimization in three-dimensional integrated circuits

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ABSTRACT

Through-silicon-via (TSV) interconnect is one of the main technologies for three-dimensional integrated circuits production (3-D ICs). Based on a parasitic parameters extraction model, first order expressions for the TSV resistances, inductances, and capacitance as functions of physical dimension and material characteristic are derived. Analyzing the impact of TSV size and placement on the interconnect timing performance and signal integrity, this paper presents an approach for TSV insertion in 3D ICs to minimize the propagation delay with consideration to signal reflection. Simulation results in multiple heterogeneous 3D architectures demonstrate that our approach in generally can result in a 49.96% improvement in average delay, a 62.28% decrease in the reflection coefficient, and the optimization for delay can be more effective for higher non-uniform inter-plane interconnects. The proposed approach can be integrated into the TSV-aware design and optimization tools for 3-D circuits to enhance system performance.

1. Introduction

The unprecedented development of computer and information technology is demanding Ultra-Large-Scale-Integrated (ULSI) circuits with increasing functionality and performance at minimum cost and power consumption. The feature size of the transistor is being aggressively scaled to meet this demand. This, in turn, has introduced some very serious problems. Interconnect effects such as signal delay, distortion, and crosstalk are the dominant factors limiting overall performance. To manage these issues, a variety of methods such as repeater insertion, shielding techniques, and wire sizing have been developed. However, the power dissipation and silicon area occupied by such repeaters increases significantly with the increase of these global interconnects [1–3]. Wire sizing optimization is relatively limited due to design rules and fabrication technologies [4,5]. An innovative design architecture is required to overcome conventional interconnect design limitations for greater performance. TSV-based 3D integration [6] is emerging as a promising solution that can form highly integrated systems by vertically stacking and connecting various active physical planes. One of the most important benefits of 3D architecture over a traditional two-dimensional (2-D) design is the reduction in global interconnects and total wire-length, thereby providing higher timing performance, lower power consumption, and larger design windows. Further, a 3-D integrated system can include multiple design disciplines (Digital, analog, RF) and disparate process technologies (SOI, SiGe, GaAs, etc.), that extend the capabilities of the 3D system, expanding the boundaries of the IC design space.

An interconnect length distribution model was derived by adopting an interconnect density function [7,8]. To evaluate the system performance of 3-D ICs, the proposed delay expression included in this 3-D interconnect model neglected the impact of TSV *RLC* parasitics. Assuming the TSV was placed into the middle of the line, Zhang et al. [9] considered the effect of a vertical via on the interconnect delay. Based on TSV-aware wire-length distribution, Kim et al. [10] investigated the impact of TSV *RC* parasitics on delay and power consumption of buffered interconnects in 3-D ICs. To deeply exploit the potential of 3D circuits, Pavlidis et al. [11] took the non-uniform characteristic impedances of inter-plane interconnects into account and proposed a timing-driven optimum TSV placement method. Then the results were extended into a more complicated architecture [12]. Xu et al. [13] addressed the issue of signal integrity caused by the non-uniform impedance characteristics of interconnects and presented redundant via insertion to improve system reliability. However, these algorithms all targeted to optimization of single performance criterion such as delay, power dissipation, or signal integrity. A comprehensive TSV placement and routing approach based on multiple performance criterion is required to simultaneously improve interconnect timing performance and system reliability.

Based on the distributed resistance, inductance, and capacitance (*RLC*) 3-D interconnects, this paper presents an approach for

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TSV insertion to minimize the propagation delay with consideration to signal reflection. The paper is organized as follows: In Section 2, a first-order model for the TSV *RLC* parameters is derived. After analyzing the dependence of the line delay and signal reflection coefficient on the length of the interconnect segment and TSV physical dimension, effective algorithms for TSV insertion are described in Section 3. Simulation results are presented in Section 4, illustrating the performance optimization that can be achieved. Finally, Conclusions are provided in Section 5.

2. Physical model of TSV

The via first solution is widely used in high-performance 3-D IC designs due to higher integrated density. The cross-section view and equivalent circuit model of a typical TSV fabricated by the TSV first approach is shown in Fig. 1, where l_{TSV} and r_{TSV} are the height and radius of the Cu TSV, respectively. t_{ox} is the thickness of the dielectric for dc isolation. w_{dep} is the width of the depletion region. The impact of the skin effect on the resistance is ignored to simplify the model. The analytical expression of the dc TSV resistance is given as

$$R_{TSV} = \frac{\rho l_{TSV}}{\pi r_{TSV}^2} \tag{1}$$

The resistivity of the conducting material is given by ρ, which is 16.8 nΩ m for a Cu based TSV.

The effective capacitance of the TSV C_{TSV} is the series combination of the accumulative capacitance C_{ox} and depletion capacitance C_{dep} as depicted in Fig. 1. Prior works in [14] and [15] though examined the capacitance of bulk 3-D silicon vias, neglected the formation of the depletion region in the bulk substrate surrounding the TSV, further leading to overestimate via capacitance. [16] included the effect of the depletion region to the capacitance extraction, but still assumed the electrical field lines from the 3-D via terminate on a cylinder surrounding the via dielectric region. To accurately predict 3-D via capacitance, an analytical expression accounting for the two important physical characteristics above is introduced by [17]

$$C_{TSV} = \alpha\beta \frac{\varepsilon_{ox}}{t_{ox} + (\varepsilon_{ox}/\varepsilon_{Si}) w_{dep}} 2\pi r_{TSV} l_{TSV} \tag{2}$$

where ε_{ox} and ε_{Si} are the oxide dielectric permittivity and the silicon permittivity, respectively. The fitting parameter α is used to adjust the capacitance based on the distance to the ground planes. The term β adjusts the via capacitance since a small component of the capacitance is contributed by the portion of via farthest from the ground plane.

According to the empirical expressions [16], the self-inductance L_{TSV} and resistance R_{TSV} for the contemporary TSV with 5 μm diameter and 20 μm length are estimated to be 10 pH and 17 mΩ, respectively. The inductance voltage drop ωL_{TSV} exceeds R_{TSV} when the rise/fall time of transmission signal higher than 2 GHz. Therefore, it is imperative to consider TSV inductive effect for gigahertz-frequency 3-D interconnects design. The inductance of the TSV is given as function of geometrical parameters of radius and length [18,19]

$$L_{TSV} = \frac{\mu_0}{4\pi}\left[2l_{TSV}\ln\left(\frac{2l_{TSV}+\sqrt{r_{TSV}^2+(2l_{TSV})^2}}{r_{TSV}}\right) + \left(r_{TSV} - \sqrt{r_{TSV}^2+(2l_{TSV})^2}\right)\right] \tag{3}$$

where μ_0 is the permeability of free space given by $4\pi \times 10^{-7}$ H m.

TSV conductance G_{TSV} is a parasitic element due to the presence of lossy silicon substrate, which has a complicated relationship with substrate conductivity, TSV capacitance, and operating frequency [20]. For simplifying the influence of 3-D TSV on interconnects, a compact *RLC* TSV model, ignoring the TSV conductance is used for interconnect performance evaluation.

3. 3-D interconnects design

The TSV is an important component of the 3-D ICs, which enables the integration of heterogeneous materials, signals, and technologies and achieves inter-plane interconnects communication. Since TSVs need to cross several physical planes, the via height in 3-D ICs is longer than that in conventional 2-D ICs, after adopting of modern substrate thinning techniques, the height of a single TSV is still about 20 μm [21,22]. Therefore, TSVs not only affect the interconnect delay significantly, but also cause signal integrity degradation due to impedance discontinuity between the wires and vias. Additionally, in 3-D ICs, interconnects routed in different planes are connected with TSVs to construct the whole signal paths, and the impedance characteristic of the inter-plane is non-uniform. As a result, traditional TSV insertion approaches that placed the via in the middle of wire inevitably lead to inaccurate delay estimation. To evaluate and enhance system performance of 3-D interconnects, it is necessary to simultaneously consider the impact of TSV location and size on interconnect timing performance and signal integrity.

3.1. Interconnect delay

Some prior timing-driven via placement algorithms are solved using the distributed Elmore delay model due to the simplicity and high fidelity of this model. However, as the interconnect

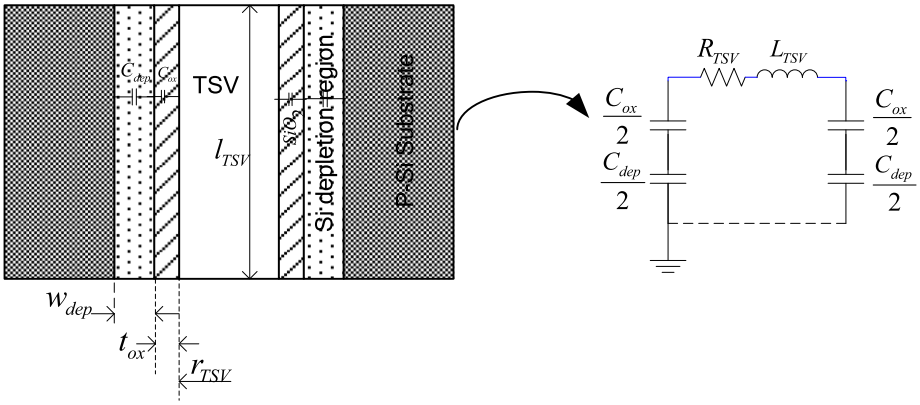

Fig. 1. The cross-section view and equivalent electrical model of a typical TSV.