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An ultra-low power integer-N frequency synthesizer for MICS transceivers

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ABSTRACT

The ultra-low power frequency synthesizer for the transceivers used in the application of Medical Implantable Communication Services (MICS) is presented. The MICS band is from 402 to 405 MHz. Each channel spacing is 300 kHz. Integer-N architecture is used to implement the frequency synthesizer. The post layout simulations show that the total power consumption of the system is less than 260 μW at 1.2 V power supply. The gains of the charge pump and voltage controlled oscillator (VCO) are 0.18 μA/rad and 50 MHz/V, respectively. The standard 300 kHz external clock is used as the reference. The design is carried out in the IBM 90 nm 9LPRF CMOS technology.

1. Introduction

Traditionally, inductive telemetry was widely used in medical diagnostics which has a very short range (10 cm max) and requires close skin contact. Since the 90s, radio frequency (RF) has been widely used in medical applications. It has numerous advantages such as increased patient safety, comfort and mobility, improvements in quality of patient care, efficiency in hospital administration capabilities and low-cost solution [1]. FCC was petitioned for the Medical Implant Communication Service (MICS) band and a spectrum was allocated with 402–405 MHz frequency range [2]. It requires monitoring and control of short-range, wireless communication channel. Many medical applications such as implantable cardioverter defibrillator (ICD), neurostimulators, cardiac pacemakers, etc are some of the medical applications which are going to use this band of interest. This new monitoring and diagnostics methodology removes limitations with the traditional short range inductive wires and the body contact [3]. However, implant battery power is limited and the impedance of implant batteries is relatively high. During communication sessions, current should be less than 6 mA for most implantable devices [4]. Furthermore, minimum external component count and minimum physical size are also important factors. Hence, very low-power consumption is the most critical criteria for such an implantable transceiver. Moreover, the low bandwidth and low amplitude nature of the physiological signals imposes different design and optimization challenges to achieve low-power consumption and miniaturization [5,6]. It is well known that in the low power wireless transceiver design, the frequency synthesizer is normally one of the main power consuming blocks and one of the most challenging blocks to integrate on chip. Reasons are the large power consumption and poor phase noise of the integrated VCO and large chip area taken by the loop filter [7,8].

In order to meet the specific low power design requirement in MICS transceivers, a very low power integer-N frequency synthesizer is designed and simulated with post-layout extraction netlist. Although sigma–delta fractional-N PLL synthesizers [9] are more agile than the integer-N structure, the latter is easily implemented and free from the fractional spurs and the out-of-band phase noise is not degraded by the quantization noise of Sigma–Delta modulator [10]. However, the larger divider ratio of the integer-N PLL will deteriorate the in-band noise performance. The high-purity crystal-oscillator can be used as the reference clock to solve the problem [11]. This low power synthesizer is composed of the following blocks as shown in Fig. 1: Phase and frequency detector (PFD), charge pump (CP), second-order low pass filter (LP), a two-stage differential ring VCO, and the frequency divider (/N). The synthesizer can generate a frequency in the range of 402–405 MHz with a 300 kHz channel spacing. The specification of every component is carefully chosen to meet the low power specification. For instance, a typical dual chamber heart pacemaker consumes less than 10 mW, lasts more than seven years on a single battery, fits in an 8 cc case and weighs less than 18 g [1].

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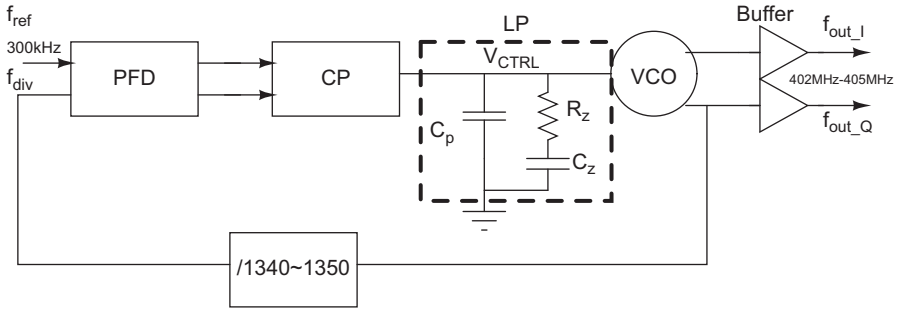

Fig. 1. Overall architecture of integer-N MICS frequency synthesizer.

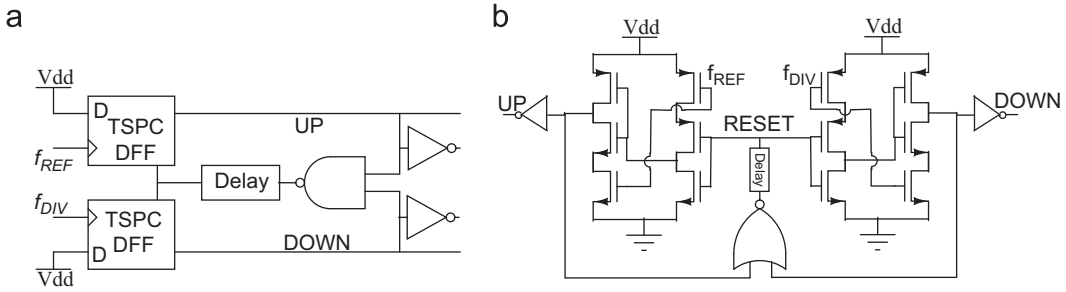

Fig. 2. (a) Block diagram of the phase-frequency detector and (b) Simplified circuit diagram as D inputs are always high.

2. The architecture of the proposed frequency synthesizer

The details of each block will be discussed in the following paragraphs.

2.1. Phase and frequency detector

The phase and frequency detector (PFD) compares the phase difference between the input reference clock and the feedback clock from the frequency divider. The conventional CMOS PFD in [12] has a large dead-zone [13] in phase characteristics at steady state which generates a large jitter in the locked state of the PLL loop. When the phase error is within the dead-zone, this feedback loop fails to correct the control voltage of the VCO. Although a nc-type PFD published in [14] has solved the dead-zone issue, the phase characteristics depend on the duty cycle of the input signals.

In this frequency synthesizer, sequential tri-state true-single-phase-clock (TSPC) D-flipflops in Fig. 2(b) are used to implement the detector. And a delay circuit element shown in Fig. 2(a) is added to the path between the NAND gate and reset so that the dead-zone is ignorable. When the input phase difference is zero or close to zero to be in the locked state, with the additional delay in the reset path, it generates a narrow and coincident pulses on both"up" and "down" signals and the reset function has sufficient time to maintain "up" and "down" pulses so that the charge pump has enough time to react. The infinitesimal increment of the phase error results in a proportional increase in the net charge accumulated in the charge pump and it is delivered to the loop filter to adjust the control voltage of the VCO. In other words, adding this delay element is essential to prevent the dead-zone problem when the input phase difference is very small. It helps the phase adjustment and reduces phase noise and timing jitter of the VCO [15]. Furthermore, for PFDs using TSPC D-flipflops, the number of gates are less than PFDs using RS-type flipflops so the power consumption is less and the operating frequency can be higher because of less gate delays in the critical reset path. The power consumption of this PFD is 98.86 nW at worst case by post layout simulation.

2.2. Charge pump

There are many discussions about different architecture of charge pumps (CP) for various PLL applications [16,17]. The non-ideal effects of the charge pumps such as leakage current, current mismatch and timing mismatch will greatly affect the phase offset error between the two input clocks of the PFD and the PLL reference spur [18,19]. In addition, the CMOS switches have non-ideal effects including charge injection, charge sharing and clock feedthrough that will cause more errors. The location of the switches such as switches at drain, gate, source or other places of the current mirrors, and single-ended or differential charge pumps have their own advantages and disadvantages in overcoming switch errors or power consumption or area occupation [20].

Combining the advantage of various architecture and compromising the power, area, error contribution of switches and switching speed, the proposed single-ended charge pump using current steering technique with switches (M_{P8},M_{P9},M_{N9},M_{N10}) in the location between current sources and cascoded transistors is shown in Fig. 3. There are several reasons to use this structure. Firstly, the current steering switch will give a faster switching speed for the charge pump which helps to reduce the settling time of the loop. Secondly, the power consumption will be less by avoiding using the active unity gain amplifier used in [21,22], while the amplifier helps to reduce the charge sharing effect when the switch is turned on. Thirdly, although the supply voltage is 1.2 V in that the cascoded transistors are working in the sub-threshold region, using cascoded current mirrors helps to increase the output impedance so that the current variation is less sensitive to the output voltage. Lastly, the location of the switches is between the cascoded transistors and current mirrors. The