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# A dual-loop shunt regulator using current-sensing feedback techniques

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The dual-loop shunt regulator using current-sensing feedback techniques is proposed in this paper. This architecture adopts a voltage and current loops to increase the transient response of the proposed shunt regulator. The maximum output current of the proposed shunt regulator is 180 mA at a 1.8 V output. Moreover the architecture of the proposed shunt regulator can suppress the stray effect which is from power supply. The prototype of the proposed shunt regulator is fabricated by the Taiwan Semiconductor Manufacturing Corporation (TSMC) 0.35-μm CMOS 2P4M process. The active area is only $579 \times 355\ \mu m^2$.



## 1. Introduction

With the ever increasing popularity of portable devices, the power supply systems determine their performance. Used for portable power management due to its simplicity of use, small board space, low noise and cost down, therefore, low-dropout regulator (LDO) has been widely used in integrated power management systems, and also outperforms switching converters. For example, in 2007, [1] adopts a current-mode feedback and voltage feedback to achieve fast transient response in a capacitor-free topology. Moreover [3] analyzes total dose exposure has been found to degrade loop gain and influence regulation, but choosing a shunt regulator topology can significantly improve reliability at higher total doses. The main drawback of linear regulators, however, is their reduced power efficiency, which is determined by dropout voltage of the pass element. LDO provides low output noise and high power efficiency with low dropout voltage of the pass device. It also shields sensitive blocks from high frequency fluctuations of the power supply and offers high accuracy, as well as fast response supply regulation [1].

Designer chooses different circuit topology to cope with different power supply control mode. Generally, power supply can be parted into two control mode: one is voltage-mode and another one is current-mode. In voltage-mode, the power supplies a fixed voltage value, designer according to the customers' desired supply voltage design functional circuit. The advantages of voltage-mode are that designer easy to tune a wanted specification and more instinctive at designed methodology. The disadvantage of voltage-mode is the noise from the power supply, and it has great influence on voltage-mode circuit. Differently, current-mode has lower noise. It hampers circuital accuracy and effectively speeds up circuital transient response [2]. The only deterred one is that current-mode is difficult to design.

These regulators use a pass element that behaves functionally like a variable resistor. Series topology is shown in Fig. 1(a), the series combination of the load resistance with the pass element forms a voltage divider to reduce the unregulated input voltage to a regulated output voltage. The other way, shunt topology is shown in Fig. 1(b), in shunt topology, the pass transistor is parallel with the load resistor and functions like a variable current divider to obtain load voltage regulation. The output voltage is sampled, scaled, and then compared with an input reference voltage. An error amplifier generates an output voltage proportional to the difference between these two voltages, which in turn biases the pass transistor through a base driver circuit. The sampling circuit and error amplifier base driver form a negative feedback loop that maintains the regulator output voltage at the desired level.

All regulator topologies studied showed performance degradation owing to total dose and single event transient radiation events. However, there are design choices that can be made to minimize these harmful effects. Total dose exposure has been found to degrade loop gain and affect regulation, but choosing a shunt regulator topology can considerably improve reliability at higher total doses. Loop gain degradation affects line regulation more directly than the control-to-output function. Total dose also has the potential to render regulators unstable by affecting high frequency performance. Single event transients striking the error amplifier disrupt the entire regulator, but again the shunt topology reacts less severely than the equivalent series topology [3]. Increasing total dose is shown to degrade converter regulation

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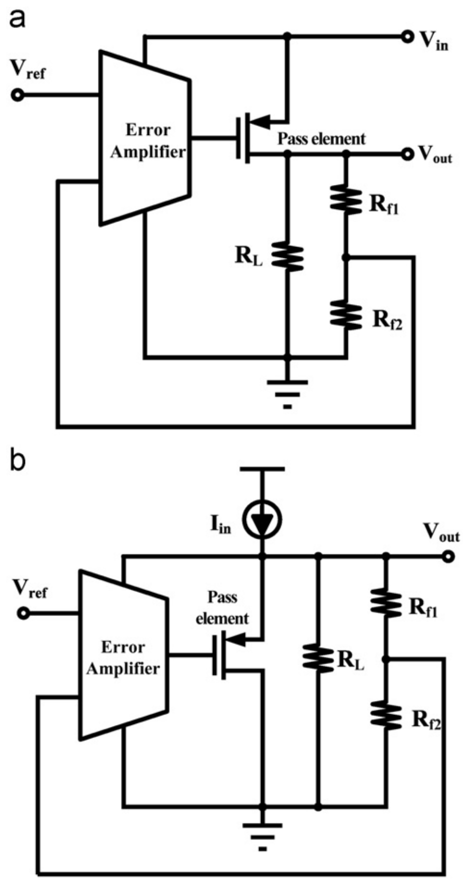


**Fig. 1.** (a) Series topologies and (b) shunt topologies.

by degrading the loop gain and phase response. Shunt regulator topologies are found to be superior to series regulator topologies in terms of radiation tolerance.

By utilizing the shunt regulator topologies, we can promote the radiation tolerance; high reverse-PSRR shunt regulators were used to close partly the noise of the digital blocks and prevent from coupling to the sensitive analog blocks, while high forward-PSRR series regulators reduce the supply injected spurs [4].

Because the SoC products decreases chip cost, stability increases; it has become more and more popular in recent decade. However, it is difficult integrating analog and digital circuits into a single chip. For the noise viewpoint, digital circuits will generate power bounce [2] and transmit noise via the power line to the analog circuits. The important parameter of accuracy signal is the ripple of power line that couple with the output of operational amplifier, phase lock loop, voltage-controlled oscillator or degrade the signal to noise ratio (SNR) of an ADC. Those usually use shunt topology to prevent stray effect of power supply. In this work, a dual feedback structure is adopted. A global voltage mode feedback achieves an accurate steady-state operation, and a secondary current feedback amplifier (CFA) is utilized to achieve fast transient response and high slew rate [1,5,6]. Based on the reasons above all, the shunt regulator is needed to implement for high-speed applications.

## 2. Circuit descriptions

Fig. 2 illustrates the block diagram which is the circuit structure of the proposed shunt regulator; the shunt regulator is supplied energy by current supply. The power supply of the controlled circuit, which are Gm- and Rm-stages, is written below as

$$V_{DDC} \cong I_{DD} \times R_{eq} \tag{1}$$

The $R_{eq}$ equals the parallel resistance of $R_L$ and $ro_n$. The proposed shunt regulator includes an operational trans-conductor amplifier Gm-stage, an operational trans-impedance amplifier Rm-stage, a current-sense circuit *M*10 and a pass element *Mn*. In this circuit, there are dual controlled paths, which are voltage controlled and current controlled paths. Voltage controlled path is the feedback of output voltage that sets the circuit stabilizing at the wanted voltage same as the reference voltage. Via the current-sensing circuit, pass element is copied a sense current, which couples into trans-impedance amplifier Rm-stage gains the extent of error [7]. The size ratio of pass element and sensing device of the design is

$$\frac{(W/L)_{Mn}}{(W/L)_{M10}} = \frac{6000/0.35}{10/0.35} = N = 600 \tag{2}$$

Moreover because of the current controlled path, its transient response is more superior to conventional LDO. The other way that can plus the transient response is increasing width of the pass element; it is an effective methodology but trade off cost [8].

The first stage circuit of proposed shunt regulator shown in Fig. 3; first stage consists of a Gm-stage which is one differential amplifier, i.e. $M1 \sim M4$. An error voltage has been compared and gained a current signal that exports to the next stage. The transform function is shown below:

$$\frac{V_1}{V_{in}}(s) = \frac{A1(2+s/\omega_{p1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \tag{3}$$

where

$$\omega_{p1} \cong \frac{gm_1}{C_E}, \quad \omega_{p2} \cong \frac{1}{(ro_2//ro_4)C_1}, \quad \omega_{z1} \cong \frac{2gm_1}{C_E} \text{ and}$$
$$A1 = gm_3 gm_2 \frac{ro_2}{gm_1}$$

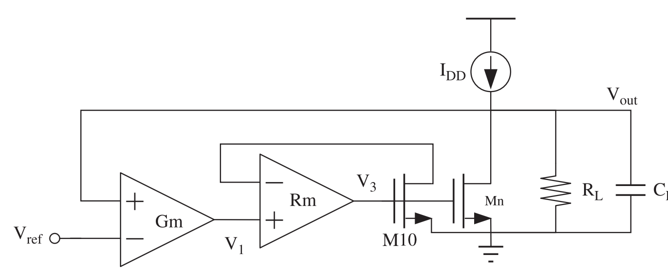


**Fig. 2.** Block diagram of the proposed shunt regulator.

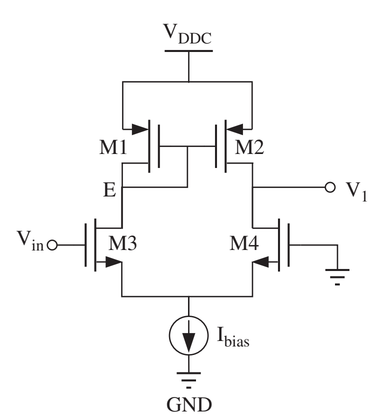


**Fig. 3.** The trans-conductor circuit Gm-stage of the proposed shunt regulator.