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900 MHz CDMA/1.8 GHz PCS/450 MHz CDMA RF receiver ICs with a new mixer linearization method and optimization of integrated inductor for single balance mixer LO buffer

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ABSTRACT

900 MHz CDMA, 1.8 GHz PCS, and 450 MHz CDMA RF receivers are implemented and measured. In order to reduce NRE cost and meet the demand of fast time-to-market, a metal-mask configurable method is applied for those receivers using only upper metals, contact and via layers. Also to reduce power consumption, a new mixer linearization method is proposed, along with an optimization methodology of an integrated inductor for a single balance mixer LO buffer, with respect to power consumption and silicon area. In order to apply the proposed inductor optimization methodology into metal-mask configurable circuits, inductor design considerations for metal-mask variant circuits are presented. With the proposed linearization technique and inductor optimization method, low power 900 MHz CDMA/1.8 GHz PCS/450 MHz CDMA mixers are obtained. The proposed receivers are fabricated in a 0.35 μm SiGe BiCMOS process. In the 900 MHz CDMA case, measurement results of the proposed mixer show 12 dBm IIP3 and 10.2 dB conversion gain, and 7.5 dB SSB NF with 10.5 mA current consumption at 2.7 V supply voltage.

1. Introduction

Currently, more and more functions are being integrated into mobile phones, which include a wide variety of multi-media functions such as, digital TV, game stations, and Internet browsing capability [1]. The mobile phone will soon evolve from a simple communication device to a complete information center in the near future. One of the main hurdles in this evolution is power consumption, which is inevitably driven upward by multi-functionality. Thus, the chip-market for mobile phone has motivated chip-makers to develop more power-efficient circuits.

In order to reduce power consumption, linearization and low noise design techniques should be employed [2,3]. A conventional active mixer, which is widely used in the wireless market, is composed of a transconductance (Gm) stage and a switching (SW) stage. Although there is a frequency conversion at the switching stage, we can regard this connection as a kind of two-stage amplifier and each stage can be optimized separately for better overall performance. However, because the Gm stage and the SW stage are directly connected in the conventional active mixer, there is no room to optimize individual performance. There have been approaches to optimize two stages separately [4,5]. However, those approaches use MOSFET for Gm stage. In a bipolar transistor case, it shows different optimization results. Here, I investigate a new mixer linearization method, treating mixer as a cascaded system.

Active mixers can be classified into single balance mixer (SBM) and double balance mixer (DBM) as shown in Fig. 1 [3]. With respect to power consumption, SBM is better than DBM, because DBM has two core circuits compared to SBM. The SBM, on the other hand, requires an integrated inductor, which occupies large silicon area at the LO buffer load to reject the IF noise from the LO buffer. The IF noise gets cancelled in the DBM due to its doubly balanced architecture [3]. The LO–IF leakage, which is the major drawback of SBM, is not considered here because I employ heterodyne architecture, which can reject LO signal with SAW filter at mixer load. As power consumption is the major criterion for mobile device, I decide to choose SBM for our design; thus, the integrated inductor design for LO buffer becomes one of the major issues. Although there have been many reported studies on application of SBM, there is a relative lack of published research on LO buffer optimization methodology with respect to low power consumption, low noise design, and integrated inductor size. Thus, even though the mixer core has small power consumption, total current including LO buffer current, is much too high [6]. Hence, in the present study, I attempt to develop an optimization methodology for an SBM LO buffer design. A brief conference paper [7] has already reported 900 MHz CDMA mixer's

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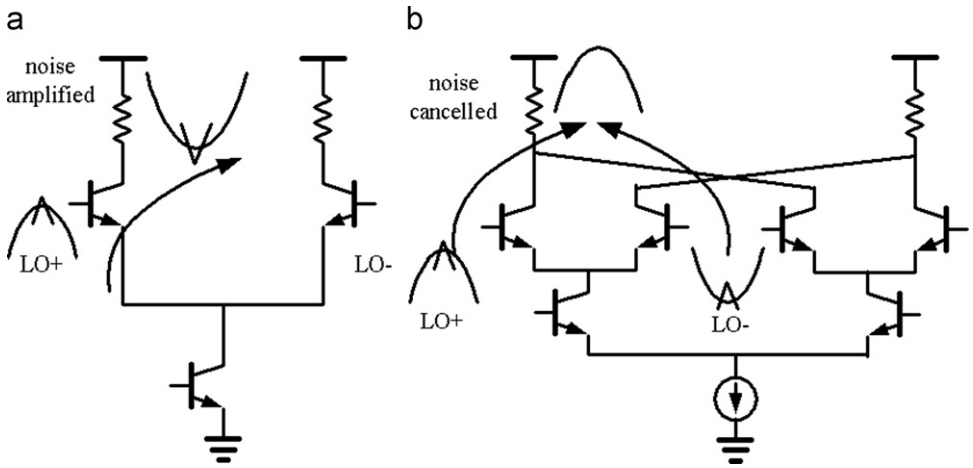

Fig. 1. (a) Single balanced mixer (SBM) and (b) Double balanced mixer (DBM). The SBM cannot reject IF noise from the LO buffer, which gets cancelled in the DBM due to its doubly balanced architecture.

performance; in this paper it discusses more details and expands its design to 450 MHz CDMA and 1.8 GHz PCS using metal-mask configurable method.

Currently, many different mobile phone standards, such as Cellular 900 MHz CDMA, 1.8 GHz PCS, Cellular 450 MHz CDMA, WCDMA, etc., are driving chip makers to integrate all standards into a single chip, such as multi-band/multi-mode chips [7,8]. However, in Korea, it is not necessary to integrate all standards in a single phone, because any one of those networks can cover the whole nation. Hence, a small size and low cost chip has greater benefits than large, high cost multi-band/multi-mode chips. In this regard, by applying the metal-mask configurable method [9,10], it is possible to fabricate multi-chips such as 900 MHz CDMA, 1.8 GHz PCS, and 450 MHz CDMA. First, I make 900 MHz CDMA receiver IC core circuits, then convert that into 1.8 GHz PCS and 450 MHz CDMA application using only contact, upper metals, and via layers. This approach can save non-recurring engineering (NRE) cost as well as development time and yield a small die size chip at low cost.

The receiver architecture for this LNA and mixer is heterodyne. So a SAW filter will be used for image rejection and IIP2 is not a concern for this receiver design.

In Section 2 of this paper, I investigate a new mixer linearization technique for cellular CDMA applications using SiGe BiCMOS technology. Section 3 discusses the optimization methodology for the integrated inductor of an SBM LO buffer. Section 4 introduces the LNA circuit design and describes the metal-mask configurable method for 900 MHz CDMA/1.8 GHz PCS/450 MHz CDMA receiver chips. Experimental results and comparisons with other results are discussed in Section 5. Finally, conclusions are presented in Section 6.

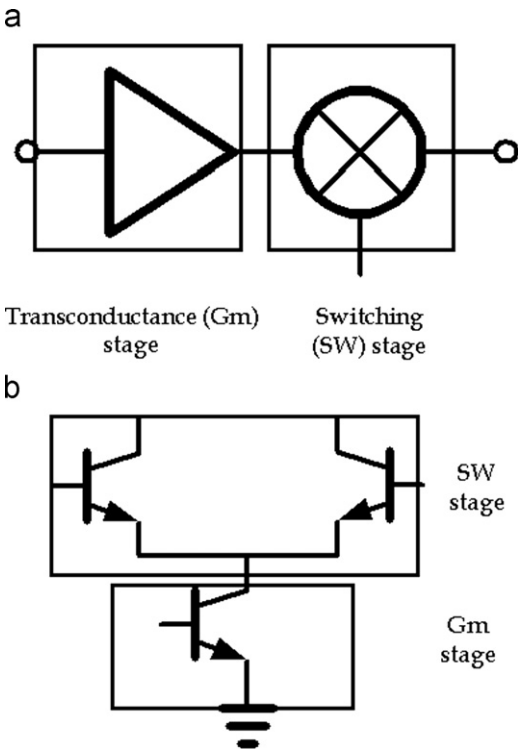

Fig. 2. (a) A conventional active mixer is composed of a transconductor (Gm) stage and a switching (SW) stage. (b) SW stage and Gm stage of SBM.

2. Mixer linearization method

A conventional active mixer is composed of a Gm stage and an SW stage, as shown in Fig. 2(a). In an SBM, the Gm stage and SW stage can be expressed as in Fig. 2(b). The Gm stage converts input voltage to current output, which is then mixed with the LO signal by the switching stage. Even though both the Gm stage and the SW stage affect linearity, the SW stage requires higher linearity than the Gm stage. As is widely known, a later stage in a cascade requires higher linearity than the preceding stage. Many previous efforts have been made to linearize the Gm stage, but those efforts do not adequately linearize the combined performance of the two stages. In particular, the SW stage is often treated as a mere switch, and thus its performance is not fully optimized. In Refs. [11,12], the high frequency SW stage linearity performance is analyzed for CMOS and bipolar transistors. The basic concept of SW stage linearity is same for both transistors. In the case of a bipolar transistor mixer, charge storage in the SW stage transistors and their base resistance affect distortion in the mixing process; thus the collector current of switching transistor and LO driving voltage are major criteria for linearity design in the SW stage. So there could be mismatch between optimum current for Gm stage and SW stage. In order to compensate the mismatch between Gm stage and SW stage, I propose using an extra current source.

SiGe bipolar transistor's linearity is well analyzed in Ref. [13]. Linearity is related with not only collector current (I_{CE}) but also