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Design of a CMOS closed-loop system with applications to bio-impedance measurements

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ABSTRACT

This paper proposes a method for impedance measurements based on a closed-loop implementation of CMOS circuits. The proposed system has been conceived for alternate current excited systems, performing simultaneously driving and measuring functions, thanks to feedback. The system delivers magnitude and phase signals independently, which can be optimized separately, and can be applied to any kind of load (resistive and capacitive). Design specifications for CMOS circuit blocks and trade-offs for system accuracy and loop stability have been derived. Electrical simulation results obtained for several loads agree with the theory, enabling the proposed method to any impedance measurement problem, in special, to bio-setups including electrodes.

1. Introduction

Impedance is a useful parameter for determining the properties of matter [1]. Today, many research goals are focused to measure the impedance of biological samples. There are several major benefits of measuring impedances in medical and biological environments: first, most biological parameters and processes can be monitored using its impedance as marker [2–5]. Second, bio-impedance measurement is a non-invasive technique and, third, it represents a relatively cheap technique in labs. Impedance Spectroscopy (IS) in cell cultures [6] and Electrical Impedance Tomography (EIT) in bodies [7] are examples of the impedance utility in this field.

For the problem of measuring a given impedance Z_x, with magnitude Z_{xo} and phase ϕ, several methods have been reported. Commonly, these methods require excitation and processing circuits. Excitation is usually done with Alternating Current (AC) sources, while processing steps are based on coherent demodulation principle [1] or synchronous sampling [8]. In both, processing circuits must be synchronized with excitation signals, as a requirement for the technique works, obtaining the best noise performance when proper filter functions (High-Pass (HP) and Low-Pass (LP)) are incorporated. Block diagrams for both are illustrated in Figs. 1 (a) and (b), respectively. The main drawback for the Ackmann method [1] is that the separated channels for in-phase and quadrature components must be matched to avoid large phase errors. Synchronous sampling proposed by Pallás avoids two channels and demodulation, by selecting accurate sampling times, and adding an HP filter in the signal path to prevent low-frequency noise and sampler interferences. Both work as feed-forward systems: the signal generated on Z_x is amplified and then processed. The setups for bio-impedance measurements usually include electrodes between their components as sensor interface between the electronic instrumentation and the bio-samples, so when excitation signals are applied, the electrodes' performance could be considered as part of the load is being excited from driving circuits point of view. A detailed description of the electrode models for biological measurement can be found in [5]. The presented work proposes a closed-loop method for bio-impedance measurement based on the AC voltage source application, with constant amplitude, to impedance under test (ZUT). This method can be applied to electrode-based sensor systems, solving the main problems of using electrodes and their impedance frequency dependence in the following forms: first, limiting by design the voltage applied to electrodes. This allows biasing the electrodes at the linear operation region. Second, it permits incorporating the frequency dependence of the electrode impedance to design equations, making easier the selection of the working frequency and allowing the optimization of the system performance, since it could be possible to set the frequency for optimum system

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response. Once these electrode constrains are considered, the proposed circuits deliver magnitude and phase impedance signals directly in easy from to be acquired: a time constant voltage, for magnitude, and the duty cycle of a digital signal, for phase.

This paper in organized as follows: Section 2 describes the proposed CMOS closed-loop system for impedance measurement. In Section 3, the main circuits employed for impedance measurement are reported. Design system considerations for loop stability are given in Section 4. Simulation results for several types of loads and setups will prove the correct performance of the proposed system in Section 5. Conclusions are underlined in Section 6.

2. Proposed impedance measure system

The proposed circuits for the measurement of impedance magnitude, Z_{xo}, consider an AC current excitation signal, with ω frequency. The circuits are designed to work maintaining a constant amplitude across the load (V_{xo}=cte), known as Potentiostat (Pstat) condition. The proposed circuit block diagram, shown in Fig. 2, has the following as main components: an Instrumentation Amplifier (IA), a rectifier, an error amplifier, and a current oscillator with programmable output current amplitude. The voltage gain of the instrumentation amplifier passband is α_{ia}. The rectifier works as a full wave peak-detector,

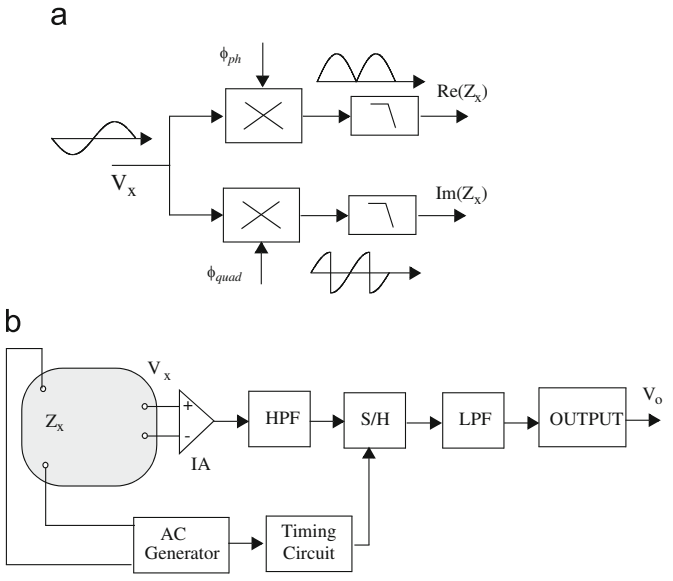

Fig. 1. (a) Coherent demodulation. (b) Synchronous sampling.

sensing the V_o peak-to-peak voltage value. Its output is a time constant voltage, V_{dc}, with α_{dc} gain ($V_{dc}=\alpha_{dc}\alpha_{ia}V_{xo}$). The error amplifier, with α_{ea} gain, will compare the DC signal with a reference, V_{ref}, to amplify the difference. The current oscillator generates the AC current to excite the load. It is composed of an external AC voltage source, V_s, an Operational Transconductance Amplifier (OTA) with g_m transconductance, and a four-quadrant voltage multiplier with K constant. The voltage generated by V_s, V_{so},sinωt, is multiplied by V_m, and current converted by the OTA. The equivalent transconductance from the magnitude voltage signal, V_m, to the excitation current, i_x, is $G_m=g_m\cdot V_{so}\cdot K$. A simple analysis of the full system gives the approximated expression for the voltage amplitude at V_x

$$V_{xo}=\frac{V_{ref}}{\alpha_{ia}\cdot\alpha_{dc}} \tag{1}$$

when condition

$$Z_{xo}G_m\alpha_{ea}\alpha_{ia}\alpha_{dc}\gg 1 \tag{2}$$

is satisfied. It is defined the system closed-loop gain as $\alpha_o=Z_{xo}G_m\alpha_{ia}\alpha_{dc}\alpha_{ea}$. Voltage in Eq. (1) remains constant if α_{ia} and α_{dc} remain constant too. Hence, Pstat condition is fulfilled if condition in Eq. (2) is true. Considering the relationship between the current i_x and the magnitude voltage V_m ($i_{xo}=G_m$, V_m), the impedance magnitude is

$$Z_{xo}=\frac{V_{xo}}{G_m}\cdot\frac{1}{V_m} \tag{3}$$

Eq. (3) shows that from voltage V_m, the impedance magnitude Z_{xo} can be calculated, since V_{xo} and G_m are known from Eq. (1) and the design parameters. The impedance phase could also be measured with V_ϕ signal in Fig. 2, by considering the input voltage oscillator, V_s, in phase with the i_x current. This signal can be squared or converted into a voltage digital signal, to be used as time reference or sync signal (V_{xd}). The V_o voltage is also converted into a squared waveform (V_{od}) by means of a voltage comparator. If these two signals feed the input of an EXOR gate, a digital signal will be obtained, V_ϕ, called phase voltage, whose duty cycle, δ, is directly proportional to the phase to be measured.

From Eq. (2), the range of Z_{xo} magnitude value must be known in order to be satisfied. However, depending of the set-up for measuring employed, the Z_{xo} can include different parasitics. In four-wire based systems, these effects are minimized by the high input impedance amplifier, but in two-wire ones, the amplifier output voltage delivers the contribution of both impedances, namely from the set-up and ZUT, so Z_{xo} must be known and quoted before to define the circuit specifications. Fig. 2 illustrates a two-wire system. The impedance to be measured should be placed between electrodes e_1 and e_2.

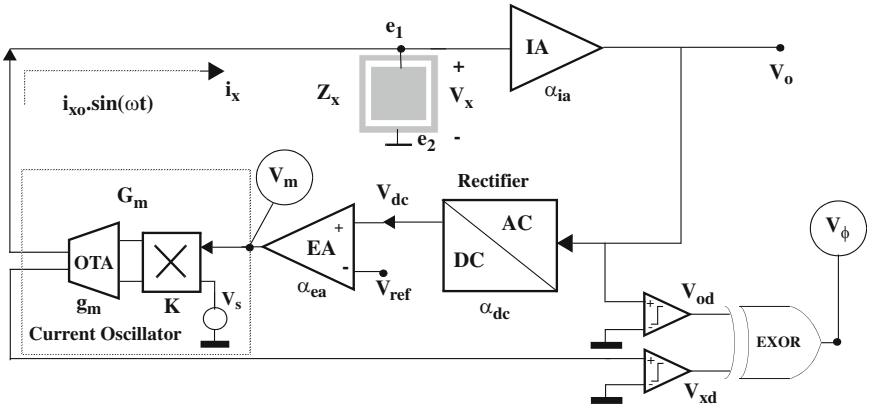

Fig. 2. Proposed circuit blocks for impedance sensing. Magnitude and phase are obtained from signals V_m and V_ϕ, respectively.