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# Prediction of thermo-mechanical integrity of wafer backend processes

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## Abstract

More than 65% of IC failures are related to thermal and mechanical problems. For wafer backend processes, thermo-mechanical failure is one of the major bottlenecks. The ongoing technological trends like miniaturization, introduction of new materials, and function/product integration will increase the importance of thermomechanical reliability, as confirmed by the ITRS (International technology roadmap for semiconductors; [1]). Since most of the thermomechanical problems initiate in the design phase, failure prevention-designing for reliability, is strongly desired. To support wafer backend process development, it is necessary to develop reliable and efficient methodologies (both testing and modeling) to predict the thermal and mechanical behavior of backend processes.

This paper presents our research results covering the backend process reliability modeling considering both thermal and mechanical (CMP) loading. The emphasis is particularly on the effect of using Cu/SiLK low-dielectric-constant (low-*k*) structure instead of the traditional Al/$SiO_2$. SiLK is a particular polymeric low-*k* material developed by the Dow Chemical Company [2] [Adv. Mater. 12 (2002) 1767].

Our results shows that Cu/SiLK structures exhibit significantly different reliability characteristics than their aluminum predecessors, and that they are more critical from several design aspects. This not only makes the stress management in the stacks more difficult, but also strongly impacts packaging.
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## 1. Introduction

The implementation of new low-*k* dielectric materials has serious consequences for the structural integrity of Cu/low-*k* interconnects. The new materials have substantially different thermo-mechanical properties than silicon oxide (TEOS), which is being used up to now as the dielectric material. Particularly, the elastic modulus of the new materials is two orders of magnitude smaller, whereas the coefficient of thermal expansion (CTE) is 20–60 times larger. Moreover, the use of copper requires a dedicated processing technique which is called damascene process. Fig. 1 shows a cross section of a simple damascene test module. The main process steps involved in making this structure are the following:

1. deposition of dielectric layers
2. patterning the dielectric (etching)
3. deposition of a diffusion barrier layer (e.g. tantalum nitride (TaN)
4. copper electroplating
5. annealing
6. planarization (chemical–mechanical polishing, CMP)

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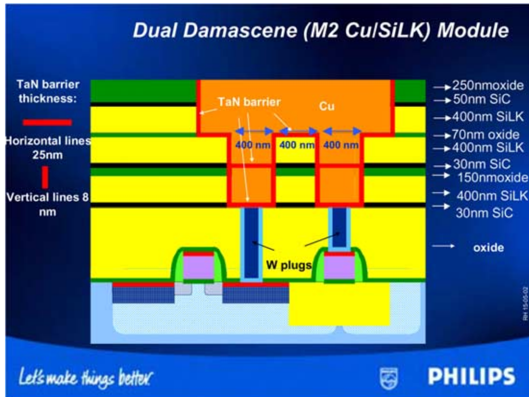


Fig. 1. Cu/low-$k$ damascene test module.

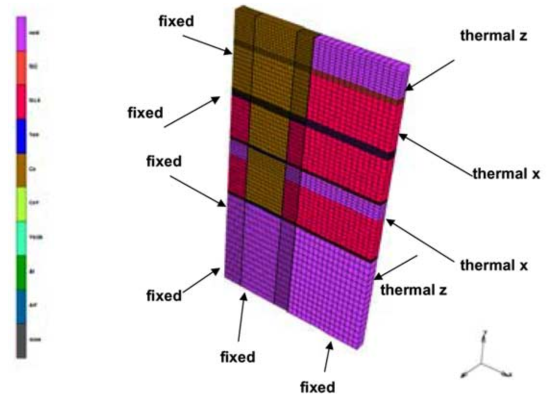


Fig. 2. Boundary conditions.

The different process steps are performed at different temperatures, and therefore the stack experiences many temperature cycles during the processing. This leads to high thermal stresses/strains, which can lead to delamination or fracture of the layers.

In this paper, we study the mechanical stresses that are introduced during the main process steps in the module sketched in Fig. 1, including the situation when a precrack is present in the stack. The finite element package Marc was used to simulate the various process steps.

## 2. Finite element analysis

The module, sketched in Fig. 1, consists of a two-level interconnect stack on a silicon wafer. To make use of the symmetry and the periodic layout, we meshed the half pitch of the module. It was assumed that the global deformations of this small part were determined by the much thicker silicon underneath.

### 2.1. Mesh

Initially a 2-D model (model 1) was made with 4-node generalized plane strain elements. Various material configurations were studied with this simple model, considering that stresses are overestimated by using plane strain conditions. Subsequently the model was expanded into the third dimension (model 2, see Fig. 2) to have a one-element thick model. Here 3-D 8-node bricks were used. The size of the meshed part is approximately $1.5 \times 3$ μm.

Modeling the process steps, mentioned earlier, required elimination (etching) and inserting (electroplating) of material. This is implemented by activating and deactivating elements. Extra elements for the barrier layer and for the copper are located 'parallel' (on the top of each other) to the elements of the dielectric layers, but they employed the same nodes, which prevented the misalignment of the mesh.

### 2.2. Boundary conditions

The boundary conditions (see Fig. 2) were set up to fulfill the symmetry and silicon driven global deformation conditions. Here the bending of the substrate and the internal force acting on the substrate can be ignored [3]. Fig. 2 illustrates the simplified model. Symmetry conditions are applied at the left-hand side of the model, as the vertical degree of freedom (DOF) was constrained. The bottom nodes are supported vertically, but can move horizontally. Coupled boundary conditions are applied at the right side of the module, where the applied deformations are calculated from the thermal expansion/shrinkage of the silicon. In case of the 3-D model, the front plane was constrained against out-of-plane deformations, and the back plane was loaded with thermal deformation.

### 2.3. Loads

The applied load for model 1 was a thermal loading, consisting of slow (isothermal) cooling down from 400 °C to room temperature (25 °C), followed by CMP loading (see later). The setup was assumed to be stress free at high temperature. In model 2, the thermal loading of the main process step was simulated. This involved various temperature cycles, as shown in Fig. 3, and the (de)activating of elements corresponding to material removal and deposition. The following sequence is repeated twice, corresponding to the processing of the two levels of the dual damascene module:

1. Deposition of carbide, SiLK, oxide layers at 400 °C
2. Cool down to RT (25 °C)
3. Etch the layers

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