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Pseudorandom signal sampler for relaxed design of multistandard radio receiver

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ABSTRACT

This paper proposes a novel software defined radio (SDR) receiver design using non-uniform sampling (NUS) technique implemented by original design of a pseudorandom signal sampler (PSS) circuit for controlling data conversion to relax multistandard receiver circuit constraints. The proposed and designed NUS-based SDR receiver allows spectral alias suppression at integer multiples of sampling frequency offering the advantages of relaxing anti-aliasing filter (AAF), reducing the analog-to-digital converter (ADC) dynamic power consumption and the automatic gain control (AGC) range as well. The PSS circuit, generating pseudorandom clock signal, with enough time-quantization accuracy, was designed. The PSS is implemented in 65-nm digital CMOS technology and occupies $470 (\mu m)^2$. It features up to 200 MHz "mean clock" for 3.2 GHz main clock while drawing 242 μ A for 1.2 V supply. Mixed experimental/simulation tests, of designed NUS-based SDR receiver, revealed a confirmation of alias-free performances and the achievement of a 72 dB (12-bit ADC) dynamic range after signal reconstruction.

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1. Introduction

Nowadays, different wireless communication networks are offering multiple services to end-users through a large choice of radio standards: Bluetooth, WiFi, WiMAX, GSM, UMTS, etc. [1,2]. Marketing success of multi-services wireless communications is depending on the feasibility of low-cost and low-power radio user terminals supporting multistandard processing with relaxed constraints on receiver circuits [3]. Software defined radio (SDR) concept is established to reach the objectives of the receiver reconfigurability, the receiver flexibility and the multi-services access, replacing stacked receivers in today used mobile handsets. SDR implementation requires a multistandard RF front-end and a software implementation of baseband processing.

Most research activities regarding SDR focus on optimizing RF receiver topologies such as homodyne, low-IF and RF subsampling [4]. SDR receiver architectures are intended to tune from 200 kHz to 20 MHz wide channels that are received from 800 MHz to almost 6 GHz [1]. However, conventional used architectures suffer from introducing high design constraints on anti-aliasing filter

manel.ben-romdhane@telecom-paristech.fr (M. Ben-Romdhane), patricia.desgreys@telecomparistech.fr (P. Desgreys), patrick.loumeau@telecom-paristech.fr (P. Loumeau), adel.ghazel@supcom.rnu.tn (A. Ghazel). (AAF) and analog-to-digital converter (ADC) in case of wideband standards [2]. In addition and due to large dynamic specification for narrow band standards and the ADC technology limits, these architectures need also to use automatic gain control (AGC) in front of the ADC [5].

In this paper, the authors propose a novel SDR receiver design using non-uniform sampling (NUS) technique implemented by original design of a pseudorandom signal sampler (PSS) circuit for controlling ADC to relax constraints of receiver circuits supporting GSM/UMTS/WiFi multistandard processing. This new idea of using NUS technique for radio signals sampling allows the main advantage of suppressing spectral aliases at integer multiples of sampling frequency produced by conventional uniform sampling technique. This reduces, for designed NUS-based SDR receiver, the constraints on the AAF, relaxes the AGC dynamic range, and decreases the ADC dynamic power consumption.

Non-uniform sampling theory and techniques are presented in various publications and used for some applications such as duty cycle measurement and spectrum analysis [6–8]. For practical implementation of NUS, some non-uniform signal sampler solutions are proposed in literature [9–16].

In works [9,11–13], non-uniform sampler design is based on chaotic oscillators implemented with discrete components. This design solution is not appropriate for monolithic integrated SDR receiver baseband stage. The second limitation is due to the generation of random continuous-time signal that needs the use of an extra component time-to-digital converter (TDC) for digital signal reconstruction in digital signal processing (DSP).



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The authors in [16] proposed an architecture which generates a time quantized signal sampler convenient for time quantized random sampling (TQ-RS) scheme and reconstruction in DSP. But the use of discrete delay component based on variable inductance lets this architecture not suitable for monolithic integrated SDR receiver baseband stage.

Solutions presented in [10,15], that generate a single continuous-time non-uniform signal (mean frequency), are not useful for multistandard that requires a variable non-uniform signal at different mean frequencies according to each standard design specifications. In addition, as solutions in [9,11–13], a TDC is required in front of digital signal reconstruction processing.

Finally, non-uniform ring oscillator proposed in [14] seems to be an interesting solution for SDR receiver baseband stage. However, this type of oscillator has an important length of inverters and depends on the chosen technology since inverter W/L CMOS parameter should be reworked to get the same inverter delay. Inverter number selection is done by a pseudorandom number generator (uniform density function). Nevertheless, the sampling periods of successive samples could overlap. This will cause a wrong sampling instant modifying the sampling point density function behavior. Hence, uniform density function is not guaranteed.

This analysis of previous work contributions permits to conclude that existing non-uniform sampler generators still present several limitations in terms of circuit integrability, variable sampling frequency, probability density function, accuracy and power consumption. To overcome these limitations, the authors propose in this paper an original circuit design of a pseudorandom signal sampler controlling the ADC to reach relaxed design for NUS-based multistandard radio receiver. Proposed PSS is designed to guarantee a better accuracy, a higher sampling frequency range, a lower power consumption and a smaller area.

The paper is organized as follows. In Section 2, NUS processing formulation and system level design of the proposed NUS-based SDR receiver are presented. Section 3 details the proposed PSS circuit design and highlights authors' contributions by comparison to previous works. In Section 4, PSS circuit digital implementation on 65 nm digital CMOS technology and mixed experimental and simulation results for the proposed NUS-based ADC control are carried out to demonstrate the advantages of the proposed NUS-based architecture and compare its performance to that achieved previously.

2. NUS-based SDR receiver design considerations

Among analog down-conversion topologies, the most adapted one for SDR processing is homodyne architecture. To illustrate the proposed design methodology, we have chosen enhanced GSM (925–960 MHz), UMTS (2110–2170 MHz) and IEEE802.11a (UNII1-2: 5.15–5.35 GHz, UNII3: 5.725–5.825 GHz) standards. Table 1 summarizes GSM/UMTS/WiFi standard specifications. The proposed design is looking forward to sharing RF front-end hardware

Table 1

GSM/UMTS/WiFi standard specifications.

Parameters	GSM	UMTS	802.11a
Channel width (MHz)	0.2	3.84	16.6
Channel spacing (MHz)	0.2	5	20
Required signal-to-noise ratio (dB)	9	6.7	26.8
Noise figure (dB)	9.8	9	10
Required ADC dynamic range (dB)	99	88.4	61.8
Required ADC resolution (bits)	17	15	10

as much as possible to reduce receiver cost, size and power consumption.

2.1. NUS processing analytical formulation

NUS process converts a continuous analog bandpass signal x(t) into its discrete representation $x_s(t)$ as indicated in Eq. (1) with $t_k < t_{k+1}$.

$$x_{s}(t) = x(t) \sum_{k=-\infty}^{+\infty} \delta(t - t_{k})$$
(1)

The sampling instant sequence $\{t_k\}$ is defined as $\{t_k, k \in Z\} \neq \{kT_s, k \in Z\}$ with T_s the mean of the sampling period. This random sequence can be defined by either jittered random sampling (JRS) [6], or additive random sampling (ARS) [7]. To obtain t_k in JRS scheme, we add a random time τ_k to deterministic instants kT_s . However, to obtain t_k in ARS scheme, we add τ_k to the previous sampling instant t_{k-1} .

If irregularities are appropriately chosen, they could provide the aliasing suppression. Alias-free processing is met when the sampling point density function assumes a constant value equal to the mean sampling frequency f_s given by Eq. (2).

$$p(t) = \sum_{k=0}^{+\infty} p_k(t) = \frac{1}{T_s} = f_s$$
(2)

where $p_k(t)$ is the probability density function of the random sampling point t_k .

This stationary condition is accomplished in case of ARS scheme, and in case of JRS scheme only for uniform probability density over $[-\frac{1}{2}T_s, \frac{1}{2}T_s]$. Nevertheless, random sampling is not convenient to generate and precisely recover uniform sampling instants [6]. In most non-uniform sampler implementations, the sampling instants are, either randomly or pseudorandomly, analogically generated. Then, these sampling generated instants are digitized before being used in digital recovering process [15].

In [8], Wojtiuk proposed the time quantized random sampling scheme. Each random time, τ_k , is quantized to $\tau_{q,k}$ and represented by Eq. (3) according to Eq. (4).

$$\tau_{q,k} = n\Delta \text{ with } \Delta = \frac{T_s}{q_T}$$
(3)

$$(n-1/2)\varDelta < \tau_k \leqslant (n+1/2)\varDelta \tag{4}$$

where q_T is the quantization time factor and n a positive integer number. The TQ-RS in case of JRS scheme for $q_T = 4$ is illustrated in Fig. 1. Wojtiuk proves that q_T should be higher than 10 to satisfy stationary condition given by Eq. (2).

To analyze these schemes behavior, a statistical parameter σ/T_s is defined to evaluate the time set randomness where σ^2 is the variance of the random time set { τ_k } or the quantized random time set { $\tau_{q,k}$ }. For alias-free sampling, we demonstrate that a suitable random scheme over $[-\frac{1}{2}T_s, \frac{1}{2}T_s]$ is characterized by $\sigma/T_s = 0.288$ [17]. Besides, in case of TQ-RS, σ/T_s depends on the quantization time factor choice.

After presenting NUS technique and particularly TQ-RS scheme, we ought to accommodate NUS to SDR receiver according to GSM/UMTS/WiFi standard specifications.

2.2. System level design of the NUS-based SDR receiver

Proposed homodyne topology for NUS-based SDR receiver is illustrated in Fig. 2. This figure shows the use of a common RF front-end for NUS- and US- based receiver. At this stage the signal is first received by a multiband antenna [18], processed by an adequate RF filter selected through an RF switch [19], and fed

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