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Temperature-adaptive voltage scaling for enhanced energy efficiency in subthreshold memory arrays

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ABSTRACT

Static random access memory (SRAM) circuits optimized for minimum energy consumption typically operate in the subthreshold regime with ultra low-power-supply voltages. Both the read and the write propagation delays of a subthreshold memory circuit are significantly reduced with an increase in the die temperature. The excessive timing slack observed in the clock period of constant-frequency subthreshold memory circuits at elevated temperatures provides new opportunities to lower the active-mode energy consumption. Temperature-adaptive dynamic supply voltage tuning (TA-DVS) technique is proposed in this paper to reduce the high-temperature energy consumption of ultra low-voltage subthreshold SRAM arrays. Results indicate that the energy consumption can be lowered by up to 32.8% by dynamically scaling the supply voltage at elevated temperatures. The impact of the temperature-adaptive dynamic supply voltage scaling technique on the data stability of the subthreshold SRAM bit-cells is presented. The effectiveness of the TA-DVS technique under process parameter and supply voltage variations is evaluated. An alternative technique based on temperature-adaptive reverse body bias (TA-RBB) to exponentially reduce the subthreshold leakage currents at elevated temperatures is also investigated. The active-mode energy consumption characteristics of the two temperature-adaptive voltage tuning techniques are compared.

1. Introduction

The embedded memory occupies the majority of the total chip area in the current state-of-the-art high-performance integrated circuits. The amount of on-chip memory is expected to continue to increase for enhancing the performance of future generations of portable devices and high-performance processors. To achieve higher reliability and longer battery lifetime in portable applications, the power consumed by the static random access memory (SRAM) arrays should be reduced. Scaling the supply voltage enhances the energy efficiency primarily by reducing the dynamic switching energy. The optimum supply voltage that provides minimum energy consumption is typically observed in the subthreshold region, as reported in [1,2].

Integrated circuits with ultra low-voltage power supplies are highly sensitive to process and temperature variations [3,7]. The absolute value of the MOSFET threshold voltage degrades and the thermal voltage is enhanced as the temperature increases [11,12]. A small increase in the die temperature exponentially enhances the subthreshold leakage current [7]. Contrary to the standard higher-voltage circuits designed for high-speed, low-voltage circuits optimized for minimum energy operate faster when the die temperature increases [4,14].

Variations in the die temperature are caused by the imbalanced switching activity and the corresponding non-uniform heat dissipation across a die and/or the fluctuations in the environmental temperature. In integrated circuits designed for minimum energy consumption, the formation of local hot-spots is unlikely on the die. The on-chip temperature gradients induced by imbalanced switching activity are therefore typically small across the die of a low-voltage integrated circuit. Die temperature fluctuations due to the variations in the ambient temperature however can cause significant fluctuations in the speed and the power characteristics of ultra low-voltage circuits. For example, the ambient temperatures for integrated circuits employed in robotic explorations vary from −180 to 486 °C [5]. Similarly, ultra low-power sensor-net modules in security applications are designed for functionality at a temperature range of −25 to 125 °C [6].

Dynamic supply voltage scaling technique is primarily used for reducing the active-mode power consumption of an integrated circuit (IC) by exploiting the variations in the computational workload [7,8]. Alternatively, adaptive body bias technique reduces both the active and the standby mode power consumption

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by dynamically adjusting the device threshold voltages depending on the variations of the workload and the circuit activity [7,9]. In this paper, a new temperature-adaptive dynamic supply voltage tuning technique is proposed for reducing the active-mode energy consumption by exploiting the excessive timing slack produced in the clock period of subthreshold SRAM circuits at elevated temperatures. The high-temperature energy efficiency is enhanced while maintaining a constant clock frequency by dynamically scaling the supply voltage of a subthreshold memory circuit with the fluctuations of the die temperature. The supply voltage that lowers the energy consumption without degrading the circuit speed at increased temperatures is identified for an SRAM array in the TSMC 180 nm CMOS technology [10]. The impact of the temperature-adaptive dynamic supply voltage scaling (TA-DVS) technique on the data stability of the subthreshold SRAM bit-cells is evaluated. The effectiveness of the TA-DVS technique under process parameter and supply voltage variations is explored. An alternative technique based on temperature-adaptive threshold voltage tuning through reverse body bias is also investigated. The active-mode energy consumption characteristics of the two temperature-adaptive voltage tuning techniques are compared.

The paper is organized as follows. The effects of temperature fluctuations on the device and circuit characteristics are examined in Section 2. The sizing constraints in a subthreshold SRAM cell and the design of a 64-bit × 64-bit ultra low-voltage SRAM array are discussed in Section 3. A methodology to identify the supply voltage providing minimum energy consumption in the standard constant-V_{DD} and constant-frequency SRAM arrays is presented in Section 4. The new temperature-adaptive supply and threshold voltage scaling techniques for dynamically reducing the energy consumed at high die temperatures are described in Section 5. The influence of the temperature-adaptive dynamic supply voltage scaling scheme on the data stability of the memory cells is examined in Section 6. The effectiveness of the TA-DVS scheme under process parameter and supply voltage variations is evaluated. Finally, some conclusions are provided in Section 7.

2. Low-voltage device and circuit behavior under temperature fluctuations

The effects of temperature fluctuations on the device and circuit characteristics are reviewed in this section. An increase in the die temperature degrades the absolute values of threshold voltage, carrier mobility, and saturation velocity of MOSFETs [4,11,12]. The saturation velocity is typically a weak function of temperature [12]. Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive $|V_{GS}-V_t|$. Alternatively, degradation in carrier mobility tends to lower the MOSFET drain current [4,13,14]. Effective variation of MOSFET drain current is determined by the variation of the dominant device parameter when the temperature fluctuates. Gate overdrive and carrier mobility variations due to temperature fluctuations at different supply voltages for devices in a 180 nm CMOS technology are listed in Table 1. Variation of the MOSFET drain current (I_{DS}) with the supply voltage and the temperature is shown in Fig. 1.

For devices operating at the nominal supply voltage ($V_{DD}=1.8$ V), variations in gate overdrive are smaller as compared to carrier mobility fluctuations when the temperature is increased from 25 to 125 °C, as listed in Table 1. The MOSFET drain current is, therefore, reduced following the degradation of carrier mobility as the temperature is increased, as shown in Fig. 1 [4,13].

The sensitivity of gate overdrive to temperature fluctuations is enhanced at scaled supply voltages, as listed in Table 1 [4,13]. For a particular lower supply voltage ($V_{DD}<1.8$ V), the temperature fluctuation induced gate overdrive variation completely counterbalances the carrier mobility variation, thereby providing temperature variation insensitive MOSFET drain current, as shown in Fig. 1 [4,13]. Further scaling of the supply voltage reverses the temperature-dependent speed characteristics of CMOS circuits. The enhanced variations of the gate overdrive voltage begin to determine the propagation delay fluctuations with the temperature. Low-voltage integrated circuits therefore operate faster when the die temperature increases [4]. When the supply voltage is scaled below the threshold voltages of the transistors, the devices operate in the weak inversion region (subthreshold regime). The switching current in the weak inversion region is the subthreshold leakage current. Subthreshold leakage current is extremely sensitive to temperature fluctuations [7]. Degradation in the device threshold voltages and the enhancement of the thermal voltage exponentially increase the subthreshold leakage currents when the die temperature increases [7].

3. Sizing of a subthreshold SRAM bit-cell

In this section, the sizing constraints for the stability and the functionality of a conventional super threshold ($V_{DD}>V_t$) SRAM cell are reviewed. The sizing constraints for the robust operation of the subthreshold SRAM circuits ($V_{DD}<V_t$) are then distinguished. The simulation setup for a 64-bit × 64-bit SRAM array is also presented.

Table 1
Gate overdrive and carrier mobility variations at different supply voltages.

Supply voltage (V)	Temperature (°C)	Gate overdrive (V)		Carrier mobility ($\times 10^{-3}$ m^2/V s)	
		PMOS	NMOS	PMOS	NMOS
1.8	25	−1.34	1.33	5.46	28.86
	125	−1.41	1.39	4.47	17.93
	Variation (%)	5.37	4.95	−18.26	−37.87
1.1	25	−0.64	0.63	6.31	35.10
	125	−0.71	0.69	5.13	20.08
	Variation (%)	11.28	10.48	−18.69	−42.78
0.7	25	−0.24	0.23	6.98	37.78
	125	−0.31	0.29	5.70	20.95
	Variation (%)	30.39	29.01	−18.36	−44.54
0.5	25	−0.04	0.03	7.39	38.66
	125	−0.11	0.09	6.06	21.25
	Variation (%)	198.88	249.31	−17.98	−45.03