Microelectronics Journal 40 (2009) 1026–1031

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A very-high output impedance charge pump for low-voltage low-power PLLs

L.-F. Tanguay *, M. Sawan, Y. Savaria

Electrical Engineering Department, Ecole Polytechnique de Montreal, Montreal, QC, Canada H3C 3A7

ARTICLE INFO

Article history:
Received 3 March 2008
Received in revised form
23 February 2009
Accepted 2 March 2009
Available online 5 April 2009

Keywords:
Charge pumps
Current mirrors
Phase-locked loops (PLLs)
Low-voltage analog CMOS design
Biomedical implants

ABSTRACT

This article presents the design of a high output compliance, very-high output impedance single-ended charge pump implemented using a new low-voltage current mirror. The output current is sampled and a feedback loop forces it to be equal to the desired reference current. This results in a very-high output impedance over a very wide output voltage range, accurate Up/Down current matching, and low transient glitches. The proposed charge pump was implemented using STMicroelectronics 1-V 90-nm CMOS process. Simulations using Spectre show that the Up/Down output currents remain constant and matched within 1% over a charge pump output voltage ranging from 119 to 873 mV. Monte Carlo process variations and mismatch simulations indicate that the $1-\sigma$ standard deviation between the Up and Down current components is 1.4 μA, or 6.8% of the nominal 20 μA charge pump current at either end of the output voltage range.

1. Introduction

With recent advances in CMOS technologies, the possibility to integrate radio-frequency (RF) circuits, baseband signal processing, and even sensors on a same chip has led to a tremendous growth of interest in the field of implantable smart medical devices and their applications [1]. Ultra-low power consumption is critical to allow using miniature batteries that would last over a long period of time. Using a nano-CMOS process for the design of the RF modules of such microsystems is appealing, since transistors offered can be operated in moderate inversion up to the GHz region, and their low threshold voltage allows designing analog circuits that can operate under 1 V. However, the shrinking of the supply voltage combined with the low output resistance of transistors in these nano-CMOS processes complicate the implementation of high output impedance current mirrors and charge pumps. Charge pumps are used in phase-locked loops (PLLs) to convert the output signal of the phase-frequency detector (PFD) into a precise quantity of charge that is either placed on or taken out of the loop-filter. Therefore, fluctuations in the loop-filter voltage due to current mismatch in the charge pump result in reference spurs in the output of the frequency synthesizer. In addition, the magnitude of the charge pump Up/Down output currents must be independent of the output voltage in order to maintain a constant loop-bandwidth and reduce the level of phase-noise in the output spectrum.

In order to eliminate Up/Down current mismatch, an operational amplifier (op-amp) in a feedback loop can be used to force the drain voltage of the output transistors to be equal to that of the reference current source [2,3]. This results in extremely precise matching between the Up and Down currents for a given output voltage, but it does not prevent the magnitude of the current from varying with the loop-filter voltage. Also, these charge pump circuits require a large and power consuming op-amp that must allow rail-to-rail operation, since current matching is maintained as long as the op-amp is in the high gain region [2]. A charge pump that uses a gain-boosting circuit to increase the output resistance of the current sources was presented in [4]. The magnitude of the current in this charge pump is determined by the ON resistance (r_{ON}) of the control switches, since they act as the reference resistance in the gain-boosting circuit. Therefore, the r_{ON} of both switches must be carefully selected and designed so that they are identical in order to avoid any mismatch in the output currents. Authors in [5] proposed a charge pump for low-voltage PLLs that combines a replica biasing technique and a feedback structure. Current matching is improved over a wide output voltage range, but the circuit is complex and power consumption is doubled due to the replica biasing scheme used.

In this paper, a novel charge pump dedicated to low-power low-voltage PLLs is proposed. The design of this circuit was motivated by the need of a nano-CMOS charge pump that would offer constant current magnitude and minimum current mismatch over a wide range of output voltage, while maintaining power consumption and complexity as low as possible. In Section 2, the operation of the new current mirror used as building blocks in the proposed charge pump is presented, followed by a description of the charge pump architecture and design.

* Corresponding author. Tel.: +1 514 340 5121; fax: +1 514 340 4147.
E-mail address: louis-francois.tanguay@polymtl.ca (L.-F. Tanguay).

0026-2692/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2009.03.001

In Section 3, simulation results are reported, and the effect of process variations and mismatch on the charge pump output current is investigated. Finally, conclusions are drawn in Section 4.

2. High output impedance charge pump using output current sampling

2.1. Enhanced low-voltage current mirror

The proposed charge pump is based on a new high output voltage compliance, high output resistance current mirror inspired from the high-swing super-Wilson current mirror presented in [6]. First, the super-Wilson and the high-swing super-Wilson current mirrors will be reviewed, then the current mirror architecture used in the proposed charge pump will be presented. The super-Wilson current mirror, shown in Fig. 1(a), achieves high output resistance by using negative feedback. The current mirror formed by M2–M4 samples the output current I_{OUT} and its value is compared with that of the input current source I_{IN}. As a result, the gate voltage of M3 is adjusted so it sinks a current equal to I_{IN}. The output resistance is directly proportional to the magnitude of the loop-gain of the feedback action from the output current to the gate of the output transistor M3. This loop-gain can be attributed to transistor M2 which, in combination with current source load I_{IN}, form a common-source amplifier used to maintain the gate voltage of output transistor M3 such that I_{OUT} is equal to I_{IN}. Due to channel-length modulation, the output current will be equal to I_{IN} only if the drain-source voltages of M2 and M4 are equal, otherwise an undesired current offset will result. In order to overcome this problem, the super-Wilson current mirror uses a diode-connected transistor M1 in series with current source I_{IN} to lower the drain voltage of M2 and make it equal to that of M4.

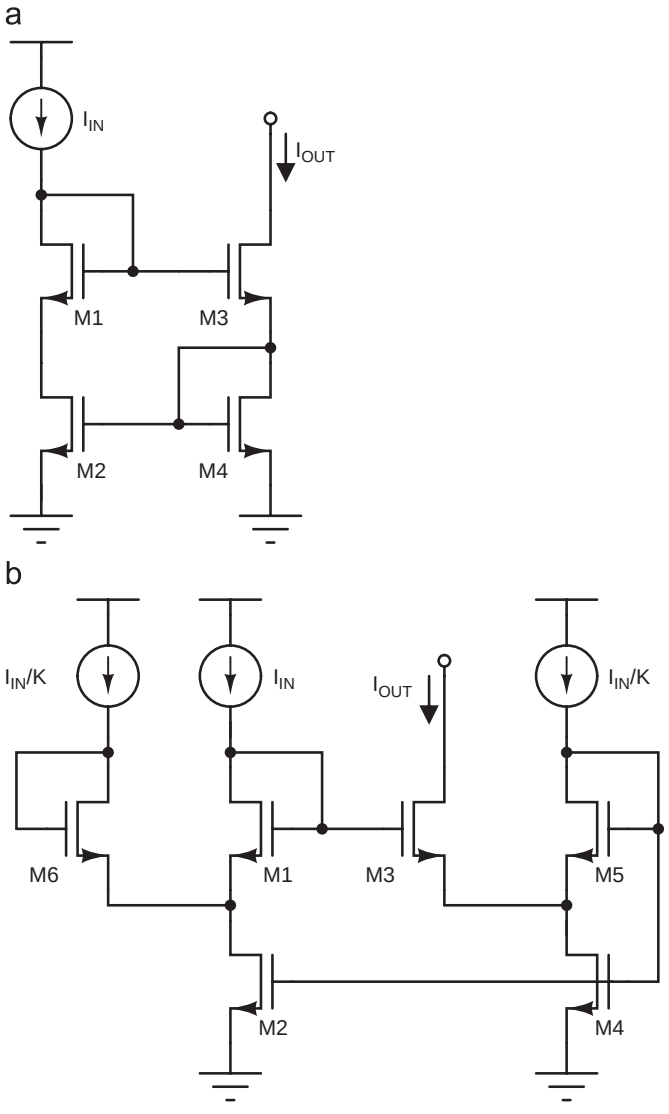

Fig. 1. CMOS implementations of (a) the super-Wilson current mirror, and (b) the high-swing super-Wilson current mirror, after [6].

The output impedance of the super-Wilson current mirror of Fig. 1(a) can be found using a test voltage source v_x at the output and finding the resulting current i_x flowing into the output port. If we assume that the output resistance of the current source I_{IN} is infinite, the effect of diode-connected transistor M1 is eliminated and the small-signal incremental output resistance $r_{out} = v_x/i_x$ is given by [7]

$$r_{out} = r_{o3}\left(1 + \frac{g_{m3}(1 + g_{m2}r_{o2}) + g_{o3}}{g_{m4} + g_{o4}}\right) \approx g_{m2}r_{o2}r_{o3} \quad (1)$$

where g_m and r_o are, respectively, the transconductance and incremental output resistance of the transistors, and g_o is their output conductance. In this equation as well as in the remaining of this paper, body effect, drain-induced barrier lowering (DIBL), and hot carriers effects are neglected for the sake of simplicity, since the goal is to give an idea on the order of magnitude of r_{out} rather than finding an exact value. The interested reader can refer to [8] for an in depth treatment of these short channel effects.

The super-Wilson current mirror has a very-high output resistance, but it requires an output voltage larger than a V_{GS} plus a saturation voltage due to the simple current sampling mirror connected in series with the output. As a result, the super-Wilson current mirror is unusable in low-supply voltage applications. The high-swing super-Wilson current mirror, shown in Fig. 1(b), solves this problem by sensing the output current with a very low input voltage current mirror that directly replaces the simple current mirror used in the super-Wilson current mirror [6]. The high-swing super-Wilson current mirror has an output compliance voltage of about two saturation voltages, and its incremental output resistance can also be approximated by (1).

In the super-Wilson and high-swing super-Wilson current mirrors presented above, the role of the diode-connected transistor M1 is to reduce unwanted offset in the output current by setting the drain of grounded transistors M2–M4 approximately to the same voltage. However, this diode-connected transistor along with the current source I_{IN} form a voltage divider from the drain of M2 to the gate of M3. Therefore, the gain of the common-source amplifier formed by M2 and I_{IN} is reduced when a non-ideal current source is used. The gain of the feedback path common-source amplifier would be significantly higher if one replaced the diode connection of transistor M1 with a cascode one, as is proposed in Fig. 2(a). By doing so, the loop-gain is increased by a factor $g_m r_o$, and so is the closed-loop output resistance of the current mirror. Therefore, assuming that the output resistance of the current sources I_{CP}/K and I_{CP} is infinite, the incremental output resistance of the proposed current mirror is given by

$$r_{out} = r_{o3}\left(1 + \frac{g_{m3}(1 + g_{m1}g_{m2}r_{o1}r_{o2}) + g_{o3}}{g_{m4} + g_{o4}}\right) \approx g_{m1}g_{m2}r_{o1}r_{o2}r_{o3} \quad (2)$$

Comparing this result with Eq. (1), we see that the proposed implementation yields to an increase of the output resistance by a factor of $g_{m1}r_{o1}$ over that of the high-swing super-Wilson current