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A CMOS piecewise curvature-compensated voltage reference

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ABSTRACT

This paper presents a novel approach to the design of a high-precision CMOS voltage reference. The proposed circuit utilizes MOS transistors instead of bipolar transistors to generate positive and negative temperature coefficient (TC) currents summed up to a resistive load to generate low TC reference voltage. A piecewise curvature-compensation technique is also used to reduce the TC of the reference voltage within a wider temperature range. The output reference voltage can be adjusted in a wide range according to different system requirements by setting different parameters such as resistors and transistor aspect ratios. The proposed circuit is designed for TSMC 0.6 μm standard CMOS process. Spectre-based simulations demonstrate that the TC of the reference voltage is 4.3 ppm/°C with compensation compared with 107 ppm/°C without compensation in the temperature ranges from −15 to 95 °C using a 1.5 V supply voltage.

1. Introduction

A voltage reference circuit is an essential part in analog and mixed-signal circuits, such as DA–AD converters, DC–DC converters, LDO regulators and so on. The most common voltage references are based on the bandgap voltage, which is obtained through parasitic bipolar transistors. Conventional bandgap reference voltage created by adding a positive temperature coefficient (TC) voltage to a negative TC voltage is given by

$$V_{\mathrm{ref}} = V_{\mathrm{BE}} + KV_{\mathrm{T}} \tag{1}$$

For silicon, the bandgap energy is approximately 1.12 eV at room temperature, which limits the minimum power supply voltage of the entire circuit to a higher value. As a result, low-voltage reference structures [1–3] and curvature-compensated techniques [4–7] are reported in much literature in recent years. Refs. [1,2] present novel approaches to low-voltage reference circuit, the supply of which is as low as 1 V. But methods in Refs. [1,2] cannot achieve a good performance of the TC. An overview of circuit techniques dedicated to low-voltage voltage references based on asymmetric differential pair has been presented in Ref. [3]. However, all of them cannot generate positive and negative TC currents, which are utilized to compensate the reference voltage. Some existing curvature-compensated architectures and techniques utilized to improve the TC of the reference voltage are proposed in Refs. [4–7]. However, all of them tend to increase the complexity and cost of circuit design by adding at least one extra operational amplifier in order to generate a negative TC current. In this paper, a high-precision voltage reference circuit, which adopts piecewise curvature-compensated technique, is proposed to overcome the above drawbacks.

2. Voltage reference circuit design

2.1. Topology of the proposed circuit

Fig. 1 shows the topology of the proposed voltage reference circuit. The positive and negative TC current generator generates a positive TC current I_{p} and a negative TC current I_{n}. The first-order temperature-independent reference voltage V_{ref1} is created by summing current I_{p} and current I_{n} up to a resistive load. The piecewise curvature-compensated block utilizes I_{p} and I_{n} to generate a compensation current, which decreases temperature drift and improves the precision of the reference voltage.

2.2. Positive and negative TC currents generator

Fig. 2 shows the circuit of the negative and positive TC currents generator, which utilizes MOS transistors instead of bipolar transistors to generate the positive and negative TC currents. The circuit on the left of the dashed line generates a positive TC current, and the circuit on the right generates a negative TC current. The operational principle is as follows [1].

The negative feedback loop composed of a high-gain operational amplifier and MOS transistors M1, M2 that have the same dimensions guarantees voltages of points A and B are equal.

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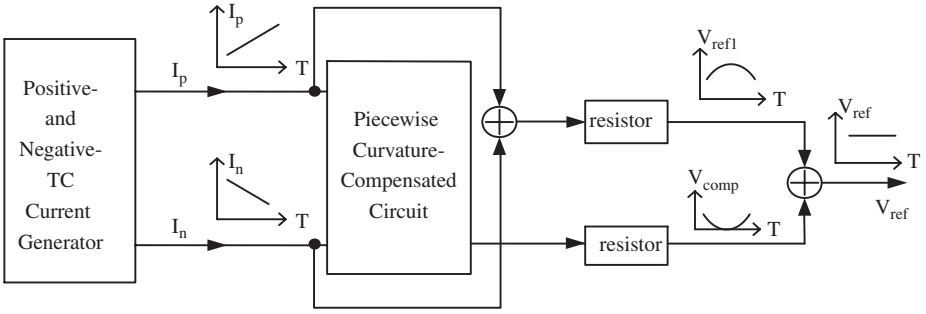

Fig. 1. The proposed circuit topology.

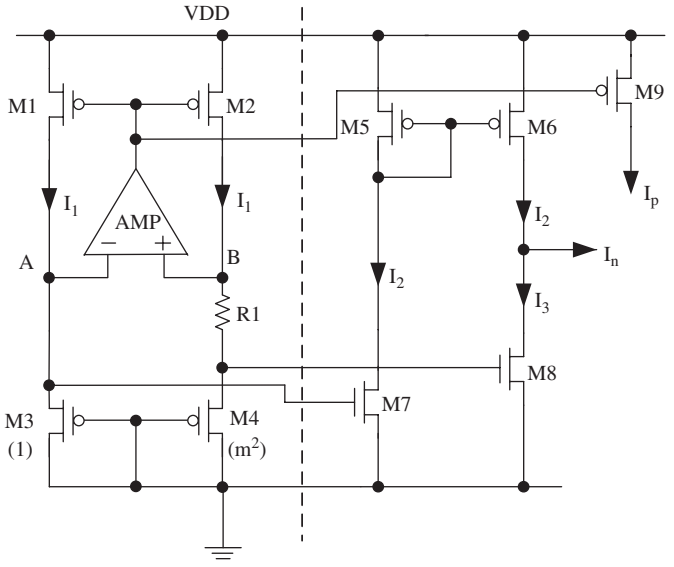

Fig. 2. Positive and negative currents generator.

As a result, an equation can be given as

$$\sqrt{\frac{2I_1}{\beta_1}} = I_1R_1 + \sqrt{\frac{2I_1}{m^2\beta_1}} \tag{2}$$

where M3 and M4 have the same dimensions, $\beta_1 = (\mu_p C_{ox}(W/L))_{M3/M4}$ and m^2 is the number of paralleled MOS transistors. From Eq. (2), the current I_p can be calculated as

$$I_p = I_1 = \frac{2}{\beta_1 R_1^2}\left(1 - \frac{1}{m}\right)^2 \tag{3}$$

Assuming $(W/L)_{M5} = (W/L)_{M6}$ and $(W/L)_{M7} = (W/L)_{M8}$. Since $V_{SG3} > V_{SG4}$, the current I_2 is larger than the current I_3. I_n can be calculated as

$$\begin{aligned} I_n &= I_2 - I_3 \\ &= \frac{2\beta_0}{\beta_1 R_1}\left(1 - \frac{1}{m}\right)^2\left\{\frac{1}{\beta_1 R_1}\left(1 - \frac{1}{m^2}\right) - (V_{thn} + V_{thp})\right\} \end{aligned} \tag{4}$$

where $\beta_0 = (\mu_n C_{ox}(W/L))_{M7}$ and $\beta_1 = (\mu_p C_{ox}(W/L))_{M3/M4}$. V_{thn} and V_{thp} are, respectively, threshold voltages of N-type transistors and P-type transistors. C_{ox} is the gate-oxide capacitor. μ_n and μ_p are mobility of N-type transistor M7 and P-type transistor M3. In most standard CMOS processes, the absolute values of V_{thn} and V_{thp} are equal and Eq. (4) can be simplified as

$$I_n \approx \frac{2\beta_0}{\beta_1^2 R_1^2}\left(1 - \frac{1}{m}\right)^2\left(1 - \frac{1}{m^2}\right) \tag{5}$$

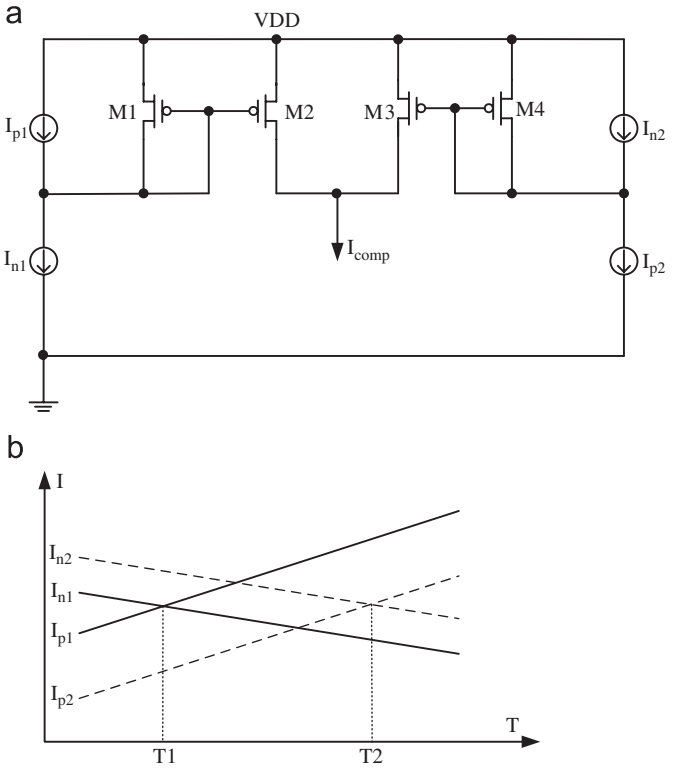

Fig. 3. (a) Piecewise curvature-compensated circuit and (b) relationships among I_{p1}, I_{p2}, I_{n1} and I_{n2}.

The relationship between mobility and temperature is expressed as follows [8]:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{\theta} \tag{6}$$

where T_0 is the reference temperature and θ is a constant, which is typically in the range of −2.0 to −1.5. So

$$\frac{\partial\mu(T)}{\partial T} = \mu(T)\frac{\theta}{T} \tag{7}$$

The TC of I_p can be derived from Eqs. (3) and (7) as follows:

$$\begin{aligned} \frac{\partial I_p}{\partial T} &= I_p\left(-\frac{1}{\mu_p}\frac{\partial\mu_p}{\partial T} - 2\frac{1}{R_1}\frac{\partial R_1}{\partial T}\right) \\ &= I_p\left(-\frac{\theta_p}{T} - 2\frac{1}{R_1}\frac{\partial R_1}{\partial T}\right) \end{aligned} \tag{8}$$

Since the positive TC (approximately +1800 ppm/°C) of the P-type diffusion resistor R1 is smaller than the negative TC (approximately −4300 ppm/°C) of hole mobility in the absolute