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New implementation of high linear LNA using derivative superposition method ☆

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ABSTRACT

New implementation of a high linear low-noise amplifier (LNA) using the improved derivative superposition (DS) method is proposed. The input stage is formed by two transistors connected in parallel. One transistor is biased in the strong inversion region as usual and another one is biased in the moderate inversion region instead of the weak inversion region, thus allowing a feasible source degeneration inductance at the sources of the two transistors to achieve a good input impedance matching and low noise figure (NF) while keeping high third-order input intercept point (IIP3) improvement with the DS method. The new implementation has been used in a 0.18-μm CMOS high linear LNA. The measured results show that the LNA achieves +11.92 dBm IIP3 with 9.36 dB gain, 2.25 dB NF and 7.5 mA at 1.8 V power consumption.

1. Introduction

Linearity is a key performance parameter for RF circuits since nonlinearity may cause harmonic generation, gain compression, desensitization, blocking, cross modulation and inter-modulation distortion, and many other problems. For the low-noise amplifier (LNA), high linearity should be achieved without lowering other performances, such as low noise figure (NF), high gain, good impedance matching and low power consumption. The linearity of the LNA is usually specified as an input-referred third-order intercept point (IIP3). Many RF systems demand higher than +8 dBm IIP3 LNAs while keeping the other performance satisfied [1]. Considering that the power supply has been lowered along with the scaling down of the feature size in the CMOS process, the high IIP3 requirement is a big design challenge and many linearization techniques are proposed to solve the problem.

The derivative superposition (DS) method [2–4], which falls under the category of feed forward, is one of the various linearization techniques. It uses two transistors connected in parallel and biased in the weak inversion region and in the strong inversion region, respectively. The sizes and bias voltages of the two transistors are chosen such that the positive peak of the third-order nonlinear coefficient of the weak inversion transistor is aligned with the negative peak of that of the strong inversion transistor. This results in an extended linear range over which the third-order nonlinear coefficient is close to zero. However, the IIP3 improvement using this method is only modest at RF (3 dB, as reported in [3]). Ref. [4] boosts IIP3 in the DS method by 10 dB by reducing the source degeneration inductance and using the cascode technique to reduce the drain load impedance. However, as reported in [1], for feasible values of the source degeneration inductance, which is limited by the downbond inductance (>0.5 nH), the conventional DS method provides no IIP3 improvement at all. But, with a very small source degeneration inductance, it is difficult to simultaneously achieve a good input impedance matching and low NF. Although the modified DS method [1] or new circuit topology [5] is proposed to boost IIP3, they need two source degeneration inductors and complicate the circuit design.

In this paper, new implementation of a high linear LNA using the improved DS method is proposed. The input stage is formed by two transistors connected in parallel. One transistor is biased in the strong inversion region and another one is biased in the moderate inversion region, thus allowing a feasible source degeneration inductance at the sources of the two transistors while keeping high IIP3 improvement with the DS method. The new implementation has been

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used in a 0.18-μm CMOS high linear LNA. The measured results verify the feasibility of the proposed implementation in improving IIP3 of the LNA.

2. Circuit description

Fig. 1 shows the principle of the DS method [2–4]. Two transistors are connected in parallel and their sources are degenerated by the same inductance L. One transistor, M_A, works in the strong inversion region as usual and another one, M_B, works in the moderate inversion region instead of the weak inversion region. Fig. 2 shows the DC I–V curve of the transistors, the vertical axis is $\ln(I_D)$ and $\mathrm{sqrt}(I_D)$, respectively. The DC I–V curve could be divided into three regions: weak inversion, moderate inversion and strong inversion. The transistor shows different I–V characteristics in different regions. The I–V curve in the weak inversion region shows exponential characteristics, while the I–V curve in the strong inversion region shows square-law characteristics. The transition region between these two regions is the so-called moderate inversion region. From Fig. 2, it could be seen that the transistor works in the moderate inversion region when V_{GS} is between 0.3 and 0.5 V.

Fig. 3 shows the third-order nonlinear coefficient G_{3A} and G_{3B} of M_A and M_B versus the voltage source V_{GS}. By setting the voltage source V_{BD} to 0.3 V, M_A is designed to work in the strong inversion region and M_B is designed to work in the moderate inversion region. G_3 is defined as

$$G_3 = \frac{1}{6}\frac{\partial^3 I_D}{\partial V_{GS}^3}$$

and controls the third-order inter-modulation distortion (IMD3) at low signal levels, thus determines IIP3. It could be seen that the third-order nonlinear coefficient G_{3A} of the transistor in the strong inversion region is negative and the third-order nonlinear coefficient G_{3B} of the transistor in the moderate inversion region is positive. The negative G_{3A} is aligned with the positive G_{3B}, but they have a similar mirror-image curvature, the resulting composite G_3 will be close to zero and the theoretical IIP3 will be significantly improved in a relatively wide range of the gate biases.

Fig. 4 shows the schematic of the whole LNA. The input stage is the same with Fig. 1, only the ESD protection circuit and the gate series inductance are added. The gate series inductance is to resonate with the gate-source capacitance of the input transistors to provide a real resistance for the input impedance matching purpose. M_A and M_B are biased by the off-chip bias voltages, V_A and V_B, to work in the strong inversion region and the moderate inversion region, respectively, so that their third-order nonlinear coefficients G_{3A} and G_{3B} reach the negative peak and positive peak. M_A and M_B could also be biased on-chip with a well-designed bias circuit. Since Fig. 3 shows that the theoretical IIP3 will be significantly improved in a relatively wide range of gate biases (about 70 mV), the accuracy requirements on V_A and V_B are not high, so it should not be very challenging to design the on-chip bias circuit. In our work, the off-chip biases are applied for the prototyping purpose.

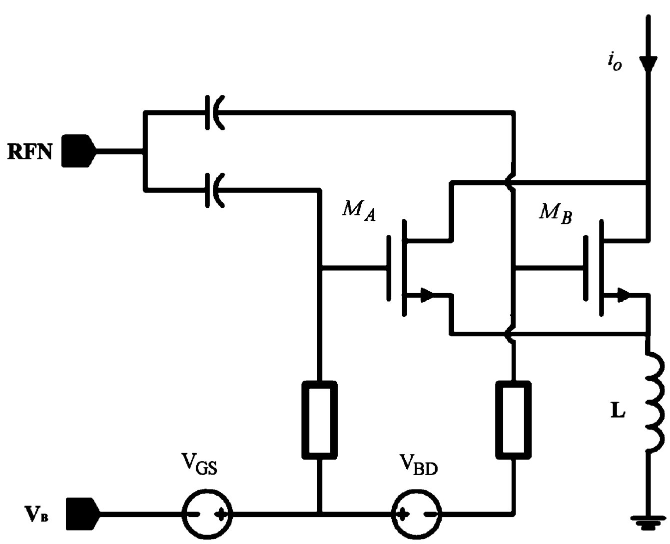

Fig. 1. Principle of the DS method.

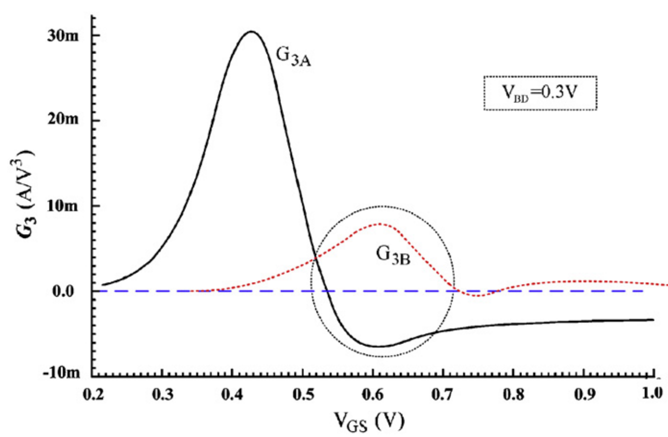

Fig. 3. The third-order nonlinear coefficient G_{3A} and G_{3B} of M_A and M_B versus the voltage source V_{GS}.

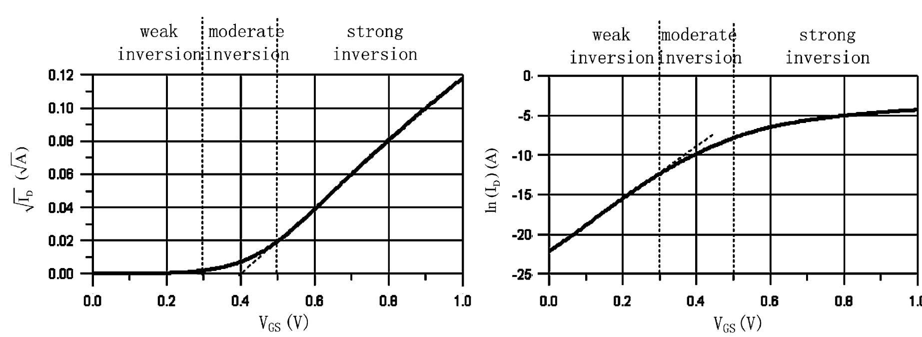

Fig. 2. The DC I–V curve of the transistors, the vertical axis is $\ln(I_D)$ and $\mathrm{sqrt}(I_D)$.