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Drive current boosting of n-type tunnel FET with strained SiGe layer at source

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Abstract

Though silicon tunnel field effect transistor (TFET) has attracted attention for sub-60 mV/decade subthreshold swing and very small OFF current (I_{OFF}), its practical application is questionable due to low ON current (I_{ON}) and complicated fabrication process steps. In this paper, a new n-type classical-MOSFET-alike tunnel FET architecture is proposed, which offers sub-60 mV/decade subthreshold swing along with a significant improvement in I_{ON}. The enhancement in I_{ON} is achieved by introducing a thin strained SiGe layer on top of the silicon source. Through 2D simulations it is observed that the device is nearly free from short channel effect (SCE) and its immunity towards drain induced barrier lowering (DIBL) increases with increasing germanium mole fraction. It is also found that the body bias does not change the drive current but after body current gets affected. An I_{ON} of $\approx 0.58\,mA/\mu m$ and a minimum average subthreshold swing of 13 mV/decade is achieved for 100 nm channel length device with 1.2 V supply voltage and 0.7 Ge mole fraction, while maintaining the I_{OFF} in fA range.

Keywords: Band-to-band tunneling; Subthreshold swing; Gated p–i–n diode; Tunnel field effect transistor (TFET); Device simulation

1. Introduction

The switching characteristics of the metal oxide semiconductor field effect transistor (MOSFET) have degraded considerably over the years due to relentless scaling. The subthreshold swing (S) of the MOSFET, which determines its switching characteristics and OFF current (I_{OFF}) is un-scalable. Due to the drift-diffusion mode of carrier transport, the S in a MOSFET is theoretically limited to a value of 60 mV/decade at the room temperature. In fact, due to various short channel effects (SCEs), punchthrough, etc., the actual value of S in the present day MOSFET is much higher, which has resulted in an increase of I_{OFF} from generation to generation and thus became a major concern for low-standby power (LSTP) applications. One therefore needs to explore novel device architectures which use other mode of carrier transport (i.e., impact ionization [1], interband tunneling [2–14], etc.) in order to achieve sub-60 mV/decade values of S. The impact ionization MOSFET (I-MOS) [1] appeared to be very promising due to its near ideal switching characteristics. However, due to problems like threshold voltage (V_{TH}) shifts caused by hot carrier injection, non-rail to rail voltage swings and high operating voltage requirements, it failed to meet the ITRS [15] requirements for LSTP application.

The tunnel field effect transistor (TFET) with perfect saturation in the output characteristics has shown a lot of promise for achieving better scaling without severe SCEs [6]. Many variants of the TFET have been proposed till date. Among them, the vertical channel tunnel FET with a strained pseudomorphic δ_{p^+} SiGe layer has been the most discussed structure. Due to its complex fabrication steps, routing (layouting) and packaging (not compatible with classical CMOS), Vertical channel TFET does not appear to be practically applicable for LSTP applications. To overcome above difficulties non-Si lateral Tunnel FET has been proposed by Baba [3] and Si lateral Tunnel FET has been proposed by Reddick [4], which enjoys CMOS compatible process steps. However, inspite of excellent

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subthreshold swing and high I_{ON}/I_{OFF} ratio, the very low I_{ON} is the main issue with this device. Recently, ON current improvement in this lateral structure has been reported using high-κ gate dielectric in a double gate structure [16]. However, it does not take into account the mobility degradation related to high-κ material, gate dielectric breakdown due to high field across the very thin high-κ material and fabrication issues related to high-κ material involved.

In this work, we propose a new classical-MOSFET-alike n-type tunnel FET architecture, which offers sub-60 mV/decade subthreshold swing with a significant improvement in I_{ON}. The enhancement in I_{ON} is achieved by introducing a thin strained SiGe layer on top of the silicon source. With the help of TCAD simulations, we have demonstrated that the proposed device is naturally immune to SCE and can be fabricated with standard CMOS process steps. It is observed that the body bias does not affect the drain current but the body current gets affected. Another original finding is that the introduction of strained SiGe layer makes the device immune to drain induced barrier lowering (DIBL) effect and the I_{ON} increases exponentially with Ge mole fraction (x). It is noted that if proposed architecture is coupled with high-κ material (as proposed in [16]) additional boost in drive current can be achieved with a thicker gate dielectric.

2. Device structure and working principle

The device being investigated is a lateral n-type tunnel FET with a strained SiGe layer on the top of the source. The tunnel FET is a gated reverse biased p^+-p-n^+ structure which uses the principle of gate controlled band to band tunneling (BTBT) for its operation. The proposed device is shown in Fig. 1. To operate the device, the p^+ source is grounded, and positive voltage (1 V) is applied to the n^+ drain with a positive sweep at gate. The working principle of conventional (without strained SiGe) TFET and band diagrams are shown in Fig. 2. In the absence of a gate voltage (non-conducting region), the tunneling barrier

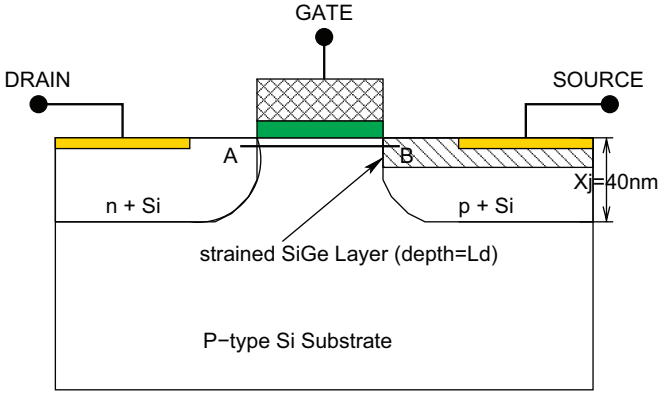

Fig. 1. Schematic of the proposed n-type TFET structure with strained SiGe layer at source. For all simulations, $t_{ox} = 2$ nm, drain doping (n^+) = 5×10^{19} and source doping (p^+) = 1×10^{20} are used.

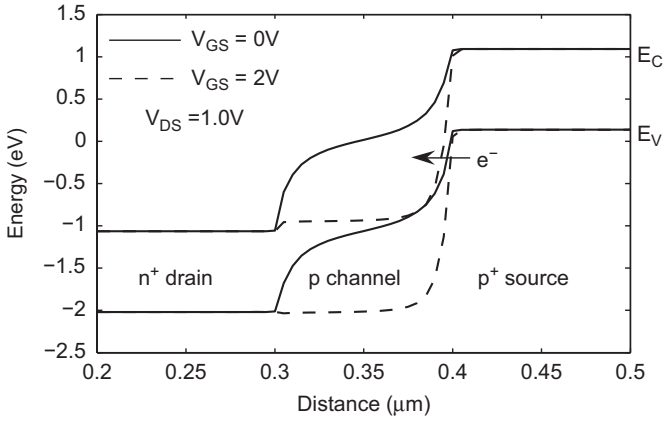

Fig. 2. Simulated band diagrams (along the cut section A–B in Fig. 1) of the n-type conventional (without strained SiGe) TFET in non-conducting and conducting regions. The large reverse biased barrier insures extremely low I_{OFF}.

width is large enough to give extremely small current (I_{OFF}). However, on application of positive gate voltage, the bands in the intrinsic (lowly doped) region are pulled downwards and a tunneling barrier is created between source and channel. Due to the reduction in tunneling width and electric fields produced, zener tunneling of electrons takes place from the valance band of the source to the conduction band of the channel and the device turns ON. One should note that this behavior is analogous to NMOS in the CMOS technology. For a tunnel FET, the ON current is proportional to the electron/hole transmission probability $T(E)$ in the BTBT mechanism, which is given by [17]:

$$T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}\right)\Delta\Phi, \quad (1)$$

where m^* is the carrier effective mass, e is the electron charge, E_g is the bandgap, $\Delta\Phi$ is the energy range over which tunneling can take place, and t_{ox}, t_{Si}, ε_{ox} and ε_{Si} are the oxide and silicon film thickness and dielectric constants, respectively. This equation shows decreasing oxide thickness (t_{ox}) [18], increasing oxide dielectric constant (ε_{ox}), and reducing bandgap (E_g), will enhance the performance of the device. Boucart and Ionescu [16] have proposed the use of high-κ materials as the gate dielectric (high ε_{ox} in Eq. (1)) in order to increase ON current (I_{ON}). In this work, I_{ON} enhancement has been done by modulating the bandgap (E_g) by using a strained SiGe layer at the source end and varying its Ge mole fraction (x). As the electron/hole effective mass m^* does not change too much with mole fraction (x), its impact on I_{ON} could be ignored.

The device performance is sensitive to the doping concentration of source and abruptness of doping profile at source-channel [9]. The doping of source, substrate and drain regions chosen to optimize I_{ON}, respectively, are 1×10^{20}, 1×10^{16} and 5×10^{19} cm^{-3}. Device performance is very sensitive to gate work function as reported in[18],