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Comparison among emission and susceptibility reduction techniques for electromagnetic interference in digital integrated circuits

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ABSTRACT

This paper presents a comparative study of susceptibility reduction techniques for electromagnetic interference (EMI) in digital integrated circuits (ICs). Both direct power injection (DPI) and very-fast transmission-line pulsing (VF-TLP) methods are used to inject interference into the substrate of a single test chip. This IC is built around six functionally identical cores, differing only by their EMI protection strategies (RC protection, isolated substrate, meshed power supply network) which were initially designed for low emission design rules. The ranking of three of these cores in terms of electromagnetic immunity is then compared with the one of their radiated emission, thanks to near-field scanning (NFS) measurements. This leads to the establishing of design guidelines for low EMI in digital ICs.

1. Introduction

Within the recent years, digital and analog integrated circuits (ICs) have been developed using a very small channel length (nanometer technology), with an increase in operating frequency and interface numbers as well as a decrease in node capacitance, power supply voltage and, consequently, noise margin. Therefore, these ICs are becoming more and more susceptible to the electromagnetic interference (EMI) induced by other ICs, antennas and, more generally, telecommunication systems. They also represent emission sources which can easily disturb other circuits located either on the same board or other boards. Therefore, a properly designed IC must bear both a low emission level and a high immunity level (i.e. ability to withstand EMI without exhibiting any malfunction). However, it may not be possible to meet both constraints at the same time.

Several measurement methods have been developed, some of them standardised, to characterise the electromagnetic emission and susceptibility of ICs. The most commonly used are summarised in Table 1.

In this paper, two of the aforementioned measurement methods (direct power injection, DPI and near-field scanning, NFS) are actually used to establish a comparison among emission levels and immunity levels of several IC cores using different power supply architectures, originally intended for emission reduction. Likewise, the susceptibility of the same IC against electrostatic discharge (ESD) is assessed using the very-fast transmission-line pulsing (VF-TLP) technique. The objective of this study is to check out whether these reduction techniques are also valid for susceptibility reduction, as well as to classify them according to their respective efficiencies and costs.

The paper is organised as follows. First of all, the different logic cores of the test chip used in this study are described in Section 2. Then, immunity measurement methods are detailed in Section 3, with an emphasis on their set-ups and their results. Section 4 deals with emission measurements. Finally, Section 5 underlines the key points of this study and opens to future research in the immunity of mixed-signal circuits.

2. Description of the test chip

The test chip used in this study, called CESAME [9], has been developed by STMicroelectronics in 0.18 μm CMOS technology (die area: 11 mm^2), specifically for the investigation of several EMI

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reduction techniques [10]. CESAME is composed of six logic cores which are identical from a functional point of view, but only differ by their power supply strategies. Each core is composed of 240 identical base cells, each one including D flip-flops, a clock tree and standard gates, intended to reflect the activity of a typical digital core. These cores are built on an epitaxial substrate with a negligible horizontal resistance.

In this paper, three cores out of the six are studied (Fig. 1).

NORM core: The only EMI protection strategy used in the NORM core consists of two small 1.7 Ω series resistors, one on each power supply rail. These resistors, along with the metal and MOS capacitances of the logic core, build up a RC filter, with a high cutoff frequency (about 200 MHz).

ISO core: Another protection strategy is used for the ISO core. This core is embedded in its own local substrate, isolated from the rest of the chip thanks to a triple-well technique (Fig. 2).

RC core: In this core, an additional 1 nF integrated decoupling capacitor is included between both supply rails (Fig. 3). This distributed on-chip capacitor is made up of several poly1/poly2 capacitors, and increases the area of the RC core by 40% compared with the NORM core. By lowering the cutoff frequency of the RC filter (about 40 MHz), this technique allows the reduction of the

Table 1
Summary of immunity and emission measurement methods for integrated circuits

Method	Upper limit (GHz)	Type	Immunity	Emission
1 Ω/150 Ω	1	Conducted	No	Yes [1]
WorkBench Faraday cage (WBFC)	1	Conducted	Yes [2]	Yes [3]
Bulk current injection (BCI)	1	Conducted	Yes [4]	No
Direct power injection (DPI)	1	Conducted	Yes [5]	No
Transverse electro magnetic (TEM) cell	1	Radiated	Yes [6]	Yes [7]
Gigahertz TEM (GTEM) cell	18	Radiated	Yes [6]	Yes [7]
Near-field scanning (NFS)	6	Radiated	Yes	Yes [8]

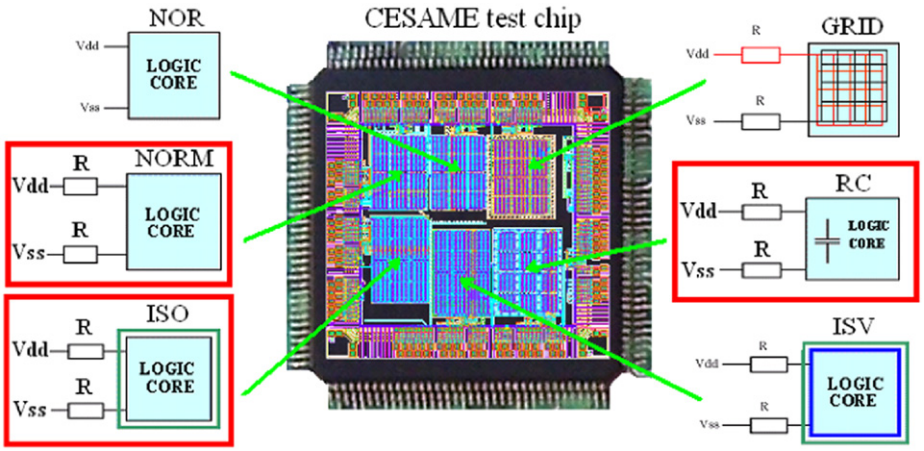

Fig. 1. CESAME test chip and the three cores under test (NORM, ISO and RC) surrounded in red.

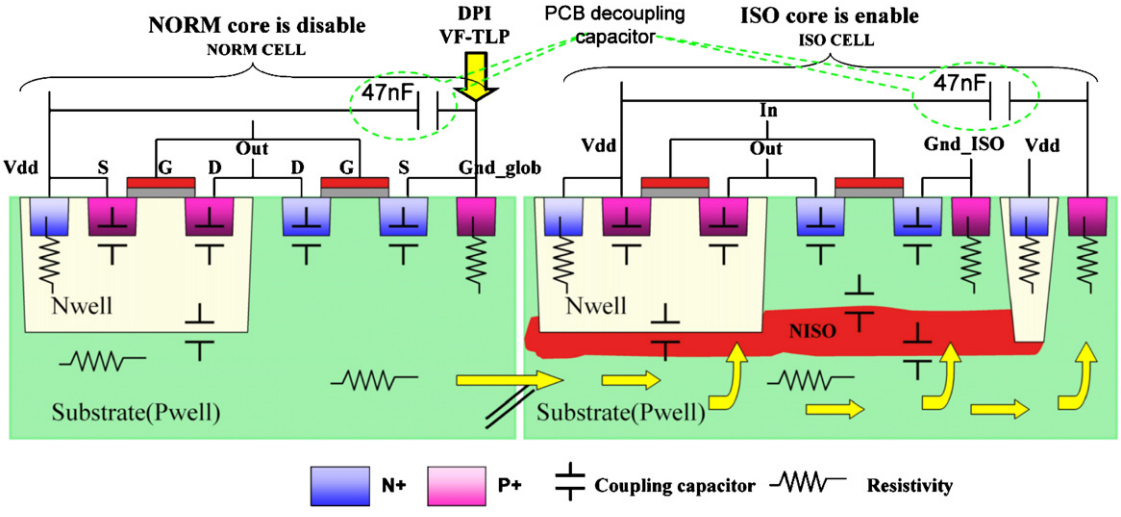

Fig. 2. Comparison between NORM and ISO core architectures.