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A novel current reference based on subthreshold MOSFETs with high PSRR

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Abstract

A novel current reference based on subthreshold MOSFETs with high power supply rejection ratio (PSRR) is presented. The proposed circuit takes full advantages of the *I–V* transconductance characteristics of MOSFET operating in the subthreshold region and the enhancement pre-regulator with the high gain negative feedback loop for the current reference core circuit. The proposed circuit, designed with the SMIC 0.18 μm standard CMOS logic process technology, exhibits a stable current of about 1.701 μA with much low temperature coefficient of 2.5×10^{-4} μA/°C in the temperature range of −40 to 150 °C at 1.5 V supply voltage, and also achieves a best PSRR over a broad frequency. The PSRR is about −126 dB at dc frequency and remains −92 dB at the frequency higher 1 MHz. The proposed circuit operates stably at the supply voltage higher 1.2 V and has good process compatibility.
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Keywords: Current reference; Voltage regulator; Low voltage; Subthreshold; CMOS integrated circuit

1. Introduction

With the development of modern electronics, there is a growing trend of designing a low-voltage high power supply rejection ratio (PSRR) current reference in many mixed-signal and analog circuits such as data converters, oscillators and PLLs [1–4]. Low-cost needs the reference to be realized in simple standard CMOS logic process technology, without resorting to the use of BiCMOS process and special devices such as floating-gate device [5,6].

Under the deep sub-micro CMOS process technique, bipolar junction transistors present several problems in the implementation of the reference circuits. The main problems include the following:

(1) The dimension does not scale down like MOSFETs.
(2) Its model parameters are usually not very well characterized.

Moreover, the current of a MOSFET operating in subthreshold region is very small and the current-mode circuit exhibits better performance than voltage-mode circuit in low-voltage conditions. So a few researchers are focusing on using MOSFETs operating in subthreshold region to design the low-voltage low-power current reference with high precision [7,8].

Recently, Filanovsky and Allam [9] studied MOSFET biased in saturation region and temperature and pointed out clearly that below a certain bias point, which depends on the technology adopted, the gate-source voltage of a MOSFET biased with a fixed drain current decreases with the temperature in a quasi-linear fashion. As a result from this observation, a gate-source voltage can be used instead of a base-emitter voltage to design a current or voltage reference independent of temperature.

This paper presents a novel CMOS current reference with the MOSFETs operating in subthreshold region to overcome the above problems. And the circuit takes advantage of the enhancement pre-regulator technique to improve the current reference supply noise performance.

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2. Gate-source voltage temperature behavior in subthreshold MOSFET

In subthreshold region, a MOSFET can be used as a bipolar transistor and the drain current I_D changes exponentially with variations in V_{GS}. The I–V transconductance characteristic of the MOSFET operating in subthreshold region is given by [10]

$$I_{ds} = n\mu C_{ox}\left(\frac{W}{L}\right)V_T^2\left[e\left(V_{gs} - V_{th}/nV_T\right)\right]\left[1 - e^{\left(-V_{ds}/V_T\right)}\right], \tag{1}$$

where C_{ox}, (W/L), V_{ds}, V_{th}, $V_T = (KT/q)$, n and μ are, respectively, the gate-oxide capacitor per unit area, the width and length ratio of MOSFET, the drain–source voltage, the threshold voltage, the thermal voltage, the slope factor and the mobility. The slope factor n can be expressed as [11]

$$n = 1 + \frac{C_{dep}}{C_{ox}} \approx 1.5, \tag{2}$$

where the C_{dep} is the surface depletion capacitor. And the mobility μ is dependent on the temperature and it is given by [12]

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m}, \tag{3}$$

where $\mu(T_0)$ is the mobility at the reference temperature T_0, and $1 \leqslant m \leqslant 2$.

When the MOSFET is used as diode-connected structure, the drain-voltage V_{ds} is much greater than the thermal voltage V_T. So the last term in Eq. (1) can be ignored. Substituting Eq. (3) into Eq. (1) to get the gate-voltage V_{gs}

$$V_{gs} = V_{th} + nV_T \ln\left[\frac{I_{ds}L}{n\mu(T_0)(T/T_0)^{-m}C_{ox}W(V_T)^2}\right]. \tag{4}$$

Assuming $m = 2$ for estimation and keeping I_{ds} constant, differentiating Eq. (4) with respect to temperature to get

$$\frac{\partial V_{gs}}{\partial T} = \frac{\partial V_{th}}{\partial T} + \frac{nK}{q}\ln\left[\frac{I_{ds}LT_0^2}{n\mu(T_0)C_{ox}W}\right]. \tag{5}$$

From Eq. (5), it can be easily seen that the term within the "ln" function is much smaller than 1, which means the second term in Eq. (5) has a negative temperature coefficient. Together with the negative temperature coefficient of the threshold voltage, so the gate-source voltage of MOSFET has a negative temperature coefficient and can be expressed as the following Equation with the first-order equivalence:

$$V_{gs}(T) = A - BT, \tag{6}$$

where $A > 0$ and $B > 0$.

3. First-order pure MOSFETs current reference circuit core

The proposed first-order pure MOSFETs current reference core circuit is shown in Fig. 1. The diode-connected

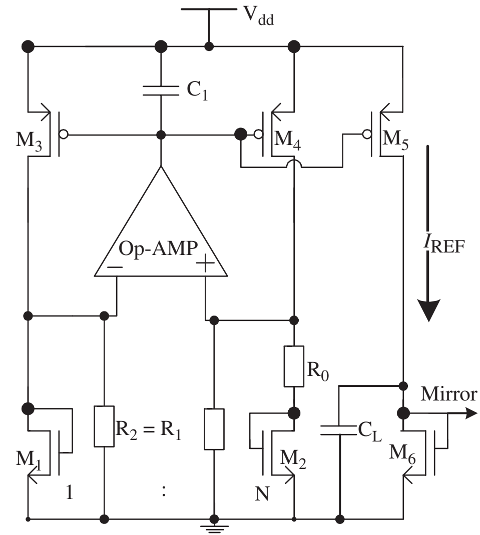

Fig. 1. The first-order current reference core circuit.

M_1 and M_2 operate in subthreshold region instead of the base-emitter junction in the convention band gap reference The op-amp forces the drain-voltage of M_3 and M_4 to be the same potential, so the currents are nominal equal in the resistance of R_1 and R_2. The capacitor C_{bypass} is a bypass capacitor to reduce the high frequency supply noise. M_6 is the output mirror transistor of the reference current. The capacitor C_L is an equivalent load capacitor.

For the length channel MOSFETs, the ratio of the width and length has very little effect on their threshold voltage. And the proportional-to-absolute current does not change the negative temperature characteristic of the subthreshold MOSFETs. Assuming $(W/L)_2/(W/L)_1 = N$, $(W/L)_3/(W/L)_4 = 1$, according to Eq. (4), the current in the resistance R_0 can be given by

$$\begin{aligned} I_{R_0}(T) &= \frac{(V_{gs,M_1} - V_{gs,M_2})}{R_0(T)}\ln\left[\frac{(W/L)_2 \times (W/L)_3}{(W/L)_1 \times (W/L)_4}\right], \\ &= \frac{nV_T}{R_0(T)}\ln N. \end{aligned} \tag{7}$$

Thus the reference current I_{REF} can be obtained as

$$\begin{aligned} I_{REF}(T) &= [I_{R_1}(T) + I_{R_0}(T)]\left[\left(\frac{W}{L}\right)_5 \Big/ \left(\frac{W}{L}\right)_4\right] \\ &= \left(\frac{V_{gs}(T)}{R_1(T)} + \frac{nV_T \ln N}{R_0(T)}\right)\left[\left(\frac{W}{L}\right)_5 \Big/ \left(\frac{W}{L}\right)_4\right]. \end{aligned} \tag{8}$$

To enhance the resistors match and process independence, all resistors are the highpoly2 resistor. According to the SMIC 0.18 μm standard CMOS logic process technology, the highpoly2 resistor is negative temperature coefficient for the first order. It can be expressed as the following equation:

$$R_{hr}(T) = R_{hr0}(T_0)1 - \lambda(T - T_0), \tag{9}$$

where the $\lambda = 5.03E - 4$ is the first-order temperature coefficient. The first-order differentiating Equation (7) with

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