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An efficient temperature dependent hot carrier injection reliability simulation flow

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ABSTRACT

This paper presents an efficient temperature dependent hot carrier injection reliability simulation flow which is scalable. The flow makes use of some efficient techniques at different design hierarchical levels to enable full chip simulation with a fast run time and high enough accuracy. While the transistor-level HCI effect is modeled based on the conventional reaction–diffusion (R–D) framework, the gate-level characterization method combines HSpice simulation and piecewise linear curve fitting to model the impact of HCI effect over the time. Also, as one of the ways to improve the speed of the simulation, only the NMOS transistors, which suffer much more from the HCI effect, are considered in the modeling. In addition, among these devices, only those which are more significantly affected are included. For each cell, only the transitions which induce the HCI impact are included. Finally, to improve the efficiency of the circuit simulation, logic cells in the circuit are classified into two groups of critical and non-critical where the critical (non-critical) ones are simulated using fine (coarse) granularity simulation time steps. The proposed method reduces the simulation time without losing much of accuracy. Also, due to the considerable impact of the temperature on the reliability, at all levels of the proposed simulation flow, the impact of the temperature on the impact of the HCI phenomena is modeled. The simulations performed on some benchmarks reveal that the proposed circuit-level HCI modeling is able to reduce the runtime of calculating the threshold voltage and mobility drifts of the gates significantly without sacrificing accuracy unacceptably. Also, the circuit-level simulations indicate an about 19% increase in the average of the HCI-induced delay degradation of the benchmarks when the temperature rises from 20 °C to 100 °C.

1. Introduction

Hot carrier injection (HCI) effect is one of the major reliability concerns in VLSI circuits. The HCI effect is a phenomenon whereby the carriers (electrons and holes) subject to a strong lateral electric field enter into the gate oxide by gaining sufficient kinetic energy (become hot enough) which enables them to overcome the potential barrier of the dielectric. It induces the generation of the interface traps at the Si/SiO_2 interface near the drain end when the gate of MOSFET switches. This effect causes unrecoverable increase in threshold voltage and decrease in the mobility parameters (i.e., V_{th} and μ, respectively) of transistors over the time [1]. The variations adversely affect the characteristics of the circuits (such as driving capability and noise margin). This effect has become more pronounced in the state-of-the-art VLSI circuits which typically utilize low supply voltage levels. The HCI impact, therefore, should be considered during the design of reliable circuits. In the case of large circuits, in addition to the accuracy of the HCI impact estimation, the efficiency is a critical concern [2].

Due to the importance of the HCI effect, there have been several works on modeling of the HCI phenomenon (see, e.g., [3,5,6,7,11,12]). One of the well-known model is reaction–diffusion (R–D) model which provides a theoretical understanding of the HCI impact [11,12]. It models the rate of the generating of hot carries proportional to the t^n where t is the operational time and n is a constant which is approximately 0.5 [11]. There is another modeling method which is called Lucky Electron Model (LEM) which is based on direct electron excitation [7]. To improve the accuracy of the LEM, an energy-driven mechanism has been proposed which is based on three different mechanisms of high-energy channel hot carriers (similar to one considered in LEM), medium energy electrons, and channel cold carriers [15,16]. The substrate current (I_{sub}) plays a major role in these methods making them rather ineffective in the nanoscale regime where other leakage current sources are also dominant [11].

Accurate modeling techniques for determining the NBTI and HCI impacts on the pMOS and nMOS transistors, respectively, have been proposed in [4]. In this work, to extract the NTBI impact, the trapping/de-trapping (TD) model (which has been widely used in BTI modeling [4,13,14]) was used while for the HCI effect, the R–D model was exploited. It should be mentioned that, in [4], the NBTI (HCI) effect has been considered for the digital (analog) circuits. In [8,9], some tools which accurately estimate the HCI impact on the performance

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degradation of the digital circuits were reported. The accuracy of the approaches originated from a proper calibration of the process technology and SPICE-like simulations. The high accuracy of these tools have been achieved at the price of very large runtimes prohibiting their use for very large circuits.

In [15], a multi-level HCI modeling technique from the cell-level to the circuit-level has been proposed. At the transistor-level, it used multi-mode energy driven model. In the cell-level, the HCI effect on the gates were modeled by considering the input slew rate and output capacitance, and its impact on the delay was stored in look-up tables (LUTs). The LUTs were used in the circuit-level to find the impact of the HCI on the circuits. An extension of this work, presented in [16], included the impact of the process variation on the HCI effect modeling. In [17] NBTI and HCI impacts on the combinational gates were studied. For modeling the HCI impact on the gates, LEM was used. Also, at the circuit-level, to model the NBTI and HCI impacts on the delay degradation of the circuit paths, a method based on the *static timing analysis* (STA) was proposed.

While the works presented in [15,16,17] generally provide accurate and efficient HCI aging analysis, they suffer from the drawback of not considering the impact of V_{th} and μ drifts on the timing behaviors of the terminal voltages during the switching transitions. Since these drifts change as the circuit ages, the impact of the HCI effect (the generation rate of the interface traps) also changes over time. In addition, note that the HCI impact is strongly temperature dependent [4,14,11], and hence, HCI-induced reliability issues should be determined by including the operating temperature in the simulation flow. None of these works has considered this dependence during the HCI circuit-level modeling.

In this work, we present an efficient a multi-level (from device-level to circuit-level) reliability simulation flow which has a fast runtime and a reasonable accuracy. The flow considers the impact of V_{th} and μ drifts on the timing behaviors of the terminal voltages. It starts from the HCI aging model based on the reaction–diffusion at the transistor-level to determine the threshold voltage and mobility shifts, continues with standard cell HCI characterization at the gate-level, and ends with full-circuit-level simulations. At the latter two levels, we suggest some techniques (such as pruning) for improving the efficiency of the simulation by reducing the runtime without reducing the accuracy unacceptably. The flow considers the operating temperature at all levels of modeling. In fact, this is one of the major modifications of this work, compared to its preliminary version presented in [10].

The details of the flow of proposed simulation framework is shown in Fig. 1 (our contributions are indicated by the check marks). Note that in this work, we selected the Reaction–Diffusion approach which was widely used for modeling the HCI impact. Apparently, one may choose other models which does not affect the proposed simulation framework except for calculating the HCI impacts on the variation of the threshold voltage and mobility. Also, since the effect of the HCI phenomenon exists when there is current flowing through the transistor (transition time) and the effect of the NBTI phenomenon manifests itself when the device is under constant gate voltage, one may consider the effects of the two phenomena separately. Hence, although we do not consider the NBTI impact on the lifetime of the circuit, its model can be incorporated in our simulation framework.

The remainder of this paper is organized as follows. Section 2 describes the R–D HCI modeling while in Sections 3 and 4, the proposed gate-level and circuit-level HCI modeling approaches are described. The results are discussed in Section 5. Finally, Section 6 concludes the paper.

2. HCI modeling based on reaction–diffusion approach

In this paper, similar to [4], the HCI impact is modeled based on the R–D framework which is an efficient and accurate approach. In this framework, the process of generating the interface traps consists of two main phases of *reaction* and *diffusion* [11,12,18]. In the standard R–D framework, the Si–H bonds at the substrate/gate oxide interface break due to the hot electrons in the reaction phase. The remaining Si dangling bond (Si*) acts as a donor-like *interface trap*, denoted by N_{it}, and the released hydrogen can diffuse away from the Si/oxide interface or anneal an existing trap. In the diffusion phase, the reaction-generated hydrogen atoms diffuse away from the interface toward the gate terminal. The generation rate of the interface traps N_{it} and the diffusion process of hydrogen atoms, are given by, respectively [11]

$$\frac{dN_{it}}{dt} = k_f(N_0 - N_{it}) - k_r N_H N_{it}, \tag{1 - a}$$

$$\frac{dN_H}{dt} = D_H\left(\frac{d^2N_H}{dx^2} + \frac{d^2N_H}{dy^2}\right), \tag{1 - b}$$

where N_0 denotes the number of the Si–H bounds at the substrate/gate oxide interface, N_H is the density of the H at the substrate/gate oxide interface, k_f and k_r are the bond-breaking and bond-annealing constants, which determine the forward and backward reaction rates, and D_H is the diffusion constant of the hydrogen atoms. By solving these equations, we can model the HCI impact during the lifetime of the transistor [11,18]. The increase in the number of traps causes

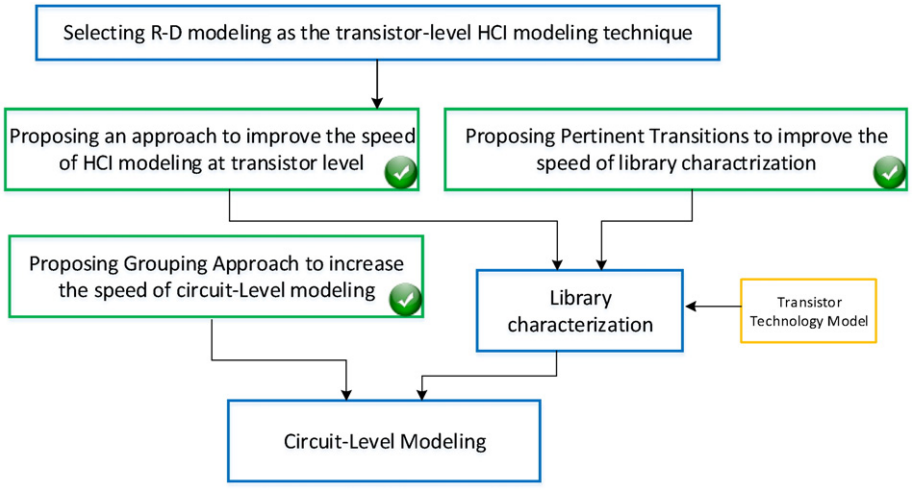

Fig. 1. The flow of proposed simulation framework (our contributions have been indicated by the check marks).