Microelectronics Reliability 57 (2016) 20–23

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Study of gate leakage mechanism in advanced charge-coupled MOSFET (CC-MOSFET) technology

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ARTICLE INFO

Article history:
Received 24 April 2015
Received in revised form 30 November 2015
Accepted 30 November 2015
Available online 4 December 2015

Keywords:
IGSS leakage
Oxide charge trapping/de-trapping
CC-MOSFET

ABSTRACT

In this work we present an alternative method to evaluate the ability to charge trap of the thermal silicon oxide grown on n^+-polysilicon in charge-coupled MOSFET devices. By interpreting the current conduction mechanism through the polysilicon-oxide by Frenkel–Poole model, we were able to evaluate and quantify the amount of charge trapped in it. We propose this approach as a very simple methodology to recognize the properties and quality of insulation of the thermal silicon oxide grown on n^+-polysilicon devices.

Contents

1. Introduction

As the demand for low power and fast switching Power MOSFET in the low-voltage wireless application is rapidly increasing, the introduction of charge-coupled MOSFET (CC-MOSFET) has enabled Si Power MOSFET technology roadmap to be further "scaled" to meet the demand [1,2]. Unlike conventional Power MOSFET where gate leakage (IGSS) current is through gate oxide, charge coupling MOSFET (CC-MOSFET) has an additional leakage path through the inter-poly oxide. CC-MOSFET devices require an additional insulation between gate and source electrodes. It is expected that the polyoxide between the two electrodes should have low leakage current and high dielectric breakdown. However it is well known that thermal oxide grown on n^+ — polycrystalline highlight a high leakage current due to the thickness uniformity [3] and local field enhancement [4–6] at the polysilicon–polyoxide interface. The electrical polyoxide properties have been shown to be largely dependent on process fabrication like poly deposition temperature doping process, and thermal oxidation method [7–8]. In this paper we analyze the transport carrier mechanism through the polyoxide layer by the Frenkel–Poole model. Using the Frenkel-Poole model we are able to find the trapped charge density into the polyoxide layer responsible of the barrier height reduction and the gate current leakage reduction after gate voltage pulse.

2. Experimental

CC-MOSFET (Area ~ 8 mm^2) device was fabricated as Fig. 1 shows. Gate oxide was thermally grown with a thickness of 47nm while inter-poly oxide layer was 150 nm. The buried n^+ poly-Si and gate electrode n^+ poly are deposited with the same recipe at 600 °C and highly doped. Together with the CC-MOSFET, a separate DUT (Area ~ 0.04 mm^2) structure was fabricated which has buried poly electrically disconnected from the source electrode as Fig. 2 shows.

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http://dx.doi.org/10.1016/j.microrel.2015.11.019
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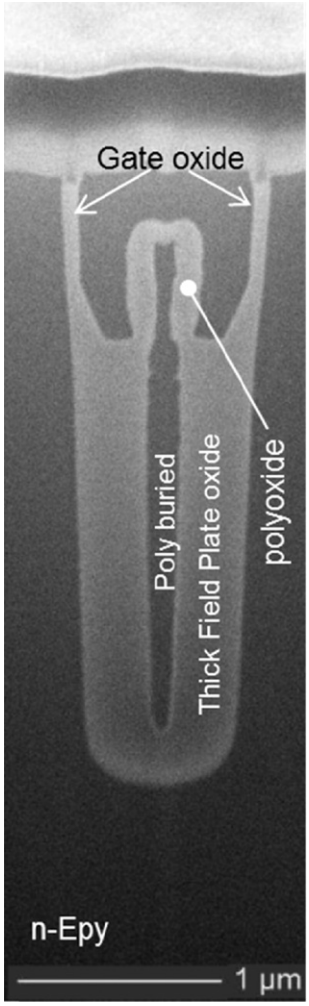

Fig. 1. Typical structure of the gate charge MOSFET device.

With this DUT, we are able to decouple the individual contribution (leakage from gate oxide or inter-poly oxide) to total leakage and subsequently, monitored by IGSS measurements.

3. Results

Fig. 3 shows the I–V characteristics of CC-MOSFET with high IGSS issue.

To decouple the dominant leakage path, further I–V characteristics were performed on the DUT (see Fig. 4).

The IGSS current was dominated by inter-poly oxide which highlights a bad insulation property. This is well-supported by the behavior of the inter-poly oxide current when a rectangular pulse signal was applied on the gate electrode. Fig. 5 shows 12 different virgin CC-MOSFETs on which we had applied a rectangular pulse signal on the gate electrode with a pulse height (from 10 V to 22 V). Every pulse reduces the IGSS and pushes the onset of tunneling leakage to higher V_{Gate} due to the charge trapped into the polyoxide.

The polyoxide leakage decreases after every rectangular pulse because the trapped charge into the polyoxide dielectric is an electrostatic shield to the electrons injected during the next pulse.

If E_{inj} is the electrical field injection without charge trapped, E_{eff} is the effective electrical field which electrons injected into polyoxide feeling due to the presence of the electrical charge trapped during the previous pulse. We can describe this effect by the equation:

$$E_{eff} = E_{inj} - \frac{qn_T}{\varepsilon_o \varepsilon_{ox}} x^*$$

where n_T is the trapped charge density, ε_o and ε_{ox} are the vacuum permittivity and the oxide dielectric constant respectively and x^* is the effective centroid of the trapped charge.

The fresh curve in Fig. 5 refers to virgin device so that we can suppose that they are initially empty, without charge trapped. The other I–Vs refer to curves which have trapped some amount of charge due to gate voltage pulse.

The main transport mechanism through the polyoxide is depicted by Frenkel–Poole model because the trapped charge is dependent from the temperature. In fact Fig. 6 shows an example of recovery of the electrical

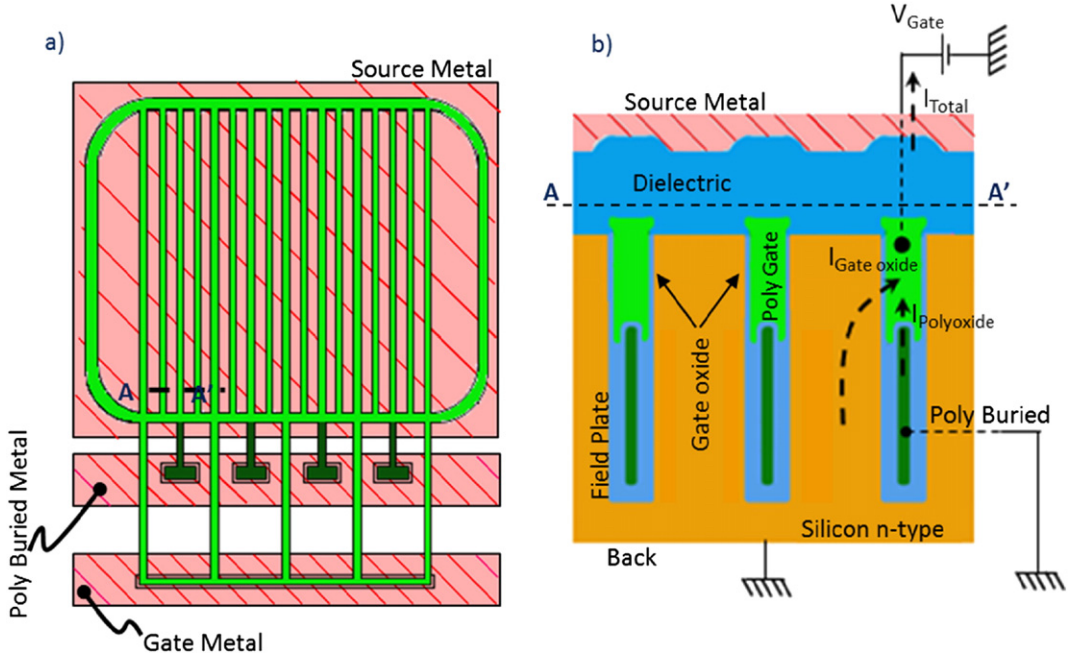

Fig. 2. The figure shows a sketch of our DUT structure layout. Panel a shows the DUT structure plan view with source, n^+ poly buried and gate metal. Panel b shows a DUT cross view along AA′ section where it is possible to see the current directions and the setup electrical configuration during an IGSS measurement.