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Improved performance of ITO/TiO_2/HfO_2/Pt random resistive accessory memory by nitrogen annealing treatment

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ABSTRACT

Resistive switching (RS) characteristics of TiO_2/HfO_2 bilayer memory devices annealed under N_2 and O_2 ambient were investigated in this work. It was found that the improved RS properties were obtained in N_2 annealing atmosphere, which exhibited good endurance of more than 100 times in direct current measurement mode and data retention properties of 10^4 s at 85 °C. To clarify the effect of annealing treatment on the devices in various atmospheres, conduction mechanism, which is related to the RS properties was analyzed. The results showed that the space charge limited current (SCLC) was the dominant conduction mechanism in HRS for the as prepared device; for the device annealed in N_2, the conduction mechanism was dominated by Pool–Frenkel emission. It can be induced that the conduction mechanism variation in N_2 was attributed to the increase of oxygen vacancies in the switching layer, which was the main reason for the improvement of RS characteristics. Lastly, we switched the operation voltage from the Pt to the ITO electrode of the double layer RRAMs, and found that better endurance and smaller operation voltages were obtained when it was applied on the Pt electrode.

1. Introduction

Conventional charge based Flash memory is approaching its physical limits due to CMOS scaling technology. Resistive random access memory (RRAM) is considered as a promising candidate for the replacement due to its simple structure, low operating consumption, high density and fast switching speed [1–4]. A typical memory device consists of an oxide layer sandwiched between metal electrodes. Normally, an electroforming process is usually needed to generate conductive filaments through the oxide layer [5,6]. Subsequently, when the electrical voltage is applied on the device, the resistance will change from high resistance state (HRS) to low resistance state (LRS), which is called SET (RESET) process.

Various materials including transition metal oxides, perovskite, and organic materials [7–10] have been reported to show resistive switching behavior. Among them, transition metal oxides HfO_2 and TiO_2, also belonging to high k materials [11], have been widely investigated due to simple composition and compatible to CMOS integrated circuit [12]. It has been reported that memory cells such as Al/TiO_2/Al and TiN/HfO_X/Pt have shown excellent performance such as ultrahigh switching speed, good switching endurance and reliable data retention [13–16]. However, recent researches on RRAMs still face challenges such as wide resistance distribution and non-uniformity of SET/RESET voltage; also, the physical mechanisms in the SET/RESET process for RRAM are still unclear [17]. For further researches on the potential applications of high k based RRAMs, the structure of the switching layer is needed to be designed to pursue excellent performance and reliability of the RRAM device [18–20]. Double layer structure RRAM is suggested to reduce switching power and improve the switching uniformity due to the stabilized formation/rupture of CFs [21–23]. For example, Philip Wong reported the multilevel capability of the TiN/HfO_X/AlO_X/Pt device by controlling the reset programming conditions [24]. Ni/GeO_X/HfON/TaN RRAM has been reported to show highly uniformity switching behavior, and low SET current of 1.6 μA and RESET current of −0.5 nA was obtained since HfON served as the charge-trapping layer, which contributed to the ultra-low switching power [25]. On the other hand, for the RRAM device, post-treatment technology is often applied to improve the performance and reliability [26]. Annealing treatment is not only adopted in CMOS technology effectively, but also a feasible and easy way to improve the device performance [27,28].

In this work, we fabricated ITO/TiO_2/HfO_2/Pt memory devices and annealed them under N_2 and O_2 ambient. The effect of annealing treatment on the resistive switching characteristics in ITO/TiO_2/HfO_2/Pt RRAMs was investigated. By comparison, we prefer to find an optimal annealing condition to improve the performance of the ITO/TiO_2/HfO_2/Pt device. The variation between the Pt and ITO operating electrodes on the resistive switching properties of the double layer RRAMs was discussed.

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2. Experimental

HfO_2 and TiO_2 films were deposited on the ITO substrate respectively by radio frequency (RF) magnetron sputtering using HfO_2 and TiO_2 targets (99.99%). Those samples were then processed with thermal annealing in N_2 and O_2 atmospheres for 30 min at 400 °C. The chamber pressure was 10 Pa and the gas flow rate was 30 cm^3/min for N_2 and O_2 respectively. A Pt top electrode of 200 nm thick was deposited with direct current (DC) sputtering using a shadow mask with an opening diameter of 100 μm. DC power of 100 W and work pressure of 5×10^{-1} Pa were used. Current–voltage (I–V) characteristics of the ITO/TiO_2/HfO_2/Pt based structure were measured at room temperature using a semiconductor parameter analyzer (Agilent B1500A).

3. Results and discussion

The forming process is usually needed to form a conductive path in the individual RRAM device prior to standard I–V measurement. Fig. 1 presents the I–V curves of the forming process for devices annealed in N_2 and O_2 atmospheres, comparing with the device without annealing treatment. The inset shows the semilog plot of the forming process. The forming voltages of as-prepared, N_2 annealed and O_2 annealed devices were 6 V, 5.1 V and 9 V, respectively. The compliance current for three samples is set to be 5 mA. It is clearly seen that the forming voltage decreased after N_2 annealing, while O_2 annealing lead to the increase of forming voltage. Based on the conductive filament theory, a conductive filament is composed of oxygen vacancies (Vo^{2+}) [29], and it will form the conductive path under a certain bias voltage. Compared with the as deposited device, O_2 annealing will result in the decrease of oxygen vacancies in the switching layer, which will lead to the increase of forming voltage for the O_2 annealed device. However, we can deduce that the amount of oxygen vacancies increased by N_2 annealing treatment for N_2 is normally regarded as a reduced atmosphere [30], which leads to the smaller forming voltage.

Fig. 2(a) presents the typical bipolar resistive switching cycles of the ITO/TiO_2/HfO_2/Pt memory devices annealed under N_2 ambient, compared with the device without annealing. Positive bias voltages from 0 V to 3 V with a 10 mA compliance current were applied after the forming process. The SET voltages for the device annealed in N_2 and the as-deposited device occurred at about 1.5 V and 1.8 V, respectively. Subsequently, when negative bias voltages were applied, the RESET voltages occurred at about −1.3 V and −1.6 V,

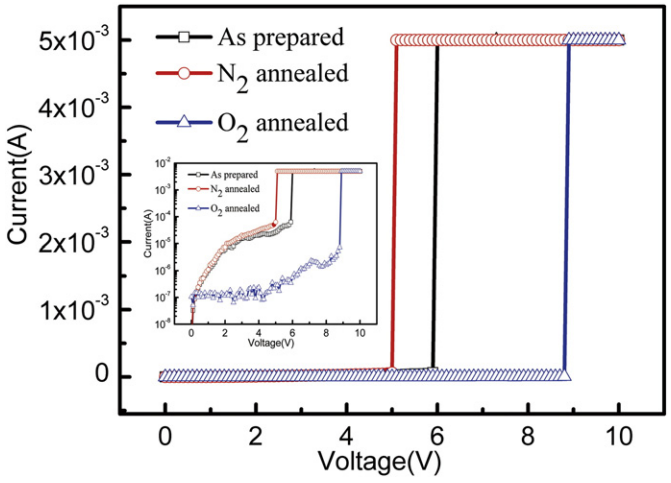

Fig. 1. I–V curves of the forming process for devices annealed under N_2, O_2 atmospheres and the as prepared sample; the inset shows the semilog plot.

as shown in Fig. 2(a). However, no SET process occurred under the voltage sweep of 0 V–3 V for the O_2 annealed device in Fig. 2(b). It is believed that oxygen vacancies or oxygen ions play a crucial role in the rupture/disrupture of the conductive filament [31,32]. The resistance of HRS increased due to the sharp decline of the Vo^{2+} concentrations for the device annealed in O_2 ambient, thus the bias voltage of 3 V was not large enough to switch the device from HRS to LRS. Fig. 2(c) and (d) shows the distributions of HRS (LRS) and SET (RESET) voltages in the probability plot [33,34] for the N_2 annealed and as prepared devices. We can find that the N_2 annealed device had a more centralized distribution of HRS (LRS) from Fig. 2(c). Also, for the device annealed in N_2, the V_{SET} maintains a clear margin and distributes in a range of 1.3–1.7 V, whereas V_{SET} for the as deposited sample shows more scattering within a wider range of 1.4–2.2 V. Therefore, it can be deduced that N_2 annealing results in more uniform resistive switching characteristics for the memory device.

Fig. 3(a) and (b) shows the endurance and retention characteristics for the N_2 annealed device, respectively. The average resistance ratio of HRS/LRS is about 60, and the resistance states are stable over 100 cycles. It is reported that the resistance ratio of HRS/LRS > 10 is required to allow for a small and highly efficient memory cell. Hence, the N_2 annealed ITO/TiO_2/HfO_2/Pt memory cell is satisfying for the application. Good retention property with a slight HRS/LRS decay for 10^4 s was measured at 85 °C. In short, N_2 is an optimal annealing condition to improve the performance of the ITO/TiO_2/HfO_2/Pt device.

To clarify the effect of annealing treatment in N_2 on the RS property in the devices, conduction mechanism was analyzed. Ohm conduction was the dominant conduction mechanism in LRS, which revealed that the conductive filament was formed in the switching layer. Fig. 4(a) shows the carrier transport mechanism in the HRS for the as deposited device and that it is dominated by a space-charge-limited current (SCLC) mechanism. While for the device annealed in N_2, the conduction mechanism changed to Pool–Frenkel emission, which is shown in Fig. 4(b). Here, we mainly discuss the electron transport mechanism, which is associated with the conduction band. By consulting other literatures [35–36], we show the conduction band diagram in the inset of Fig. 4(a) and (b). For the SCLC mechanism, shallow traps were gradually filled by electrons at the lower electric field. With the increase of the electric field, all traps are occupied and then the injected electrons will surpass the barrier under the high electric field, which leads to the sharp increase of the current. As shown in the inset of Fig. 4(b), for the Pool–Frenkel emission mechanism, which is associated with trap and field assistant currents, it is dominated by traps or oxygen vacancies existing in the switching layer, and can emit electrons from the traps under the electric force [36]. From the different conduction mechanisms for the two devices, which were shown as Pool–Frenkel emission in N_2 and SCLC emission for the as deposited sample, it can be deduced that more oxygen vacancies (Vo^{2+}), acting as the traps in the switching layer, result in the PF mechanism; while for the as deposited sample, less oxygen vacancies caused the transition of PF mechanism to SCLC mechanism. That is to say, the N_2 annealing treatment is beneficial for creating more oxygen vacancies (Vo^{2+}), which is decisive to the forming/disconnection of CF for the device. In fact, this result agrees well with the decrease of the forming voltage for the N_2 annealed device, which has been analyzed in Fig. 1. Although we cannot determine how much Vo^{2+} increased in the RRAM device after N_2 annealing when it is operating, the result is that the redox reaction that determines the formation of the localized conducting filament is easier to form, so $V_{SET/REST}$ decreased, which has been compared above. Therefore, we can conclude that the performance of the RRAM has been improved after N_2 annealing treatment which may be attributed to the increase of oxygen vacancies in the switching layer [37].