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ESD protection for negative charge pump (CP) using CP internal switches

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ABSTRACT

The standard ESD protection schemes are not very reliable for negative charge pump used in Class G power amplifiers. This work presents a novel ESD protection scheme using internal charge pump switches as ESD clamps. Transmission line pulsing (TLP) measurements show that an elevated level of ESD protection can be achieved with this scheme.

1. Introduction

Class G power amplifiers (PAs) are used in audio applications for their better power efficiency. These amplifiers use charge pumps (CPs) to switch supply voltages from ±0.5VDDA to ±VDDA to track the amplitude of the PA signal. CP switches are sensitive to ESD hazard as they are directly connected across output pads. Also, dealing with negative voltages makes it hard to use standard ESD protection schemes. In this paper, we propose an integrated ESD scheme using CP internal switches as ESD clamps for area-efficient and robust ESD protection. The design was fabricated in a TSMC 65 nm process using 2.5 V devices with 2.2 V VDDA supply voltage.

2. Background

Class G power amplifiers [4,8] are increasingly used in portable devices for their greater power efficiency over traditional Class AB power amplifiers. The Class G PA architecture is shown in Fig. 1, where a CP is used to change the supply voltage of the PA between ±0.5VDDA and ±VDDA depending on the PA input signal swing as shown in Fig. 2. The ±0.5VDDA and ±VDDA power supply modes are called Half Gain and Full Gain modes, respectively. When PA signal swing is small, the power supply voltage is set to ±0.5VDDA and once the signal crosses a predetermined threshold, the power supply is switched to ±VDDA. The switchable positive and negative voltage supplies are called VPOS and VNEG, respectively.

The charge pump design [1,3,6], shown in Fig. 3, consists of six switches that are all connected across pads. These switches are turned on using internal clocked drivers to generate different VPOS/VNEG values for different CP gain settings.

In Full Gain mode, the charge pump operates using two phases. In Phase 1, switches M1, M3 and M4 are turned on to charge VPOS and the CFLY capacitor to +VDDA. In Phase 2, switches M2 and M5 are turned on to flip the polarity of CFLY and connect it VNEG to generate −VDDA.

In Half Gain mode, CP has three phases. In Phase 1, switches M1 and M6 are connected to charge the CFLY capacitor to (VDDA–VPOS). In Phase 2, switches M3 and M4 are connected to charge CFLY to (VPOS–VSSA) which, in steady state, makes VPOS = 0.5VDDA. In Phase 3, switches M2 and M5 are turned on to flip the polarity of CFLY and connect it to VNEG to generate −0.5VDDA.

To minimize power loss and CP output resistance, use large widths for switches M1 to M6. Fig. 4 shows the plot of CP output resistance vs. frequency. At low frequencies, CP output resistance is given by 1 / (f * C) which is a standard equation for on-resistance of a switched-capacitor (SC) circuit. However, at high frequencies on-resistance is limited by switches on-resistance due to incomplete charge/discharge in each cycle. This causes on resistance to saturate beyond a critical frequency, which is approximately 500 kHz for this circuit. To keep switching power loss low while achieving minimum on-resistance for CP, circuits are operated near the critical frequency (e.g., 500 kHz in Fig. 4).

Typically, the switch width is in the order of 10 s of mm. Therefore, they cannot have drain extension (or ballasting), because it would cause an excessive increase in die area. For this process 1.4 μm minimum drain ballasting was recommended by the foundry. The channel length for a 2.5 V nominal device was 0.28 μm for this process and adding 1.4 μm drain ballasting would lead to a significant increase in area for these devices. Without ballasting, these devices are

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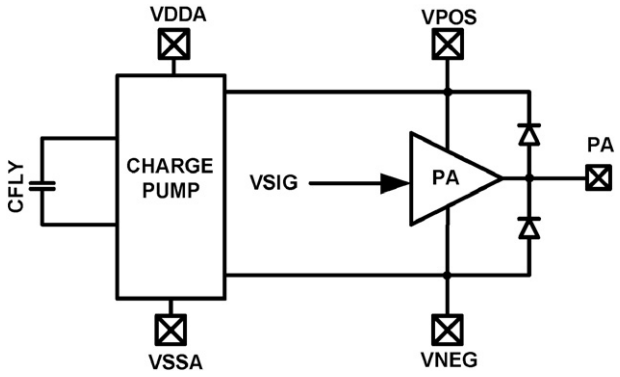

Fig. 1. Class G power amplifier architecture with charge pump to control the supply voltages.

susceptible to snap-back failure during HBM discharges unless a safe alternate low-resistance ESD discharge path is provided.

3. Standard HBM ESD protection

A standard ESD protection scheme using dual-diodes [5] and supply clamp cannot be used directly while dealing with negative voltages. An example of the standard ESD scheme is shown in Fig. 5. The entire ESD scheme is divided into positive and negative sections. The positive section comprises pins VPOS, C1P, VDDA and VSSA. The protection for these pins can be normal dual-diode based protection with an ESD clamp from supply and ground. The negative section comprises pins C1N and VNEG. A standard ESD scheme would require an ESD clamp between VSSA and VNEG and a diode between VNEG and C1N to connect the positive section to the negative section and complete the ESD discharge paths.

A closer look at the ESD scheme shows two problems. First, CP switch M5 connected between C1N and VNEG has a long discharge path through a diode and two ESD clamps, which makes this device susceptible to snap-back induced failure as it lacks drain ballasting. Second, the ESD clamp connected between VSSA and VNEG has a leakage problem when VNEG switches from −0.5VDDA to −VDDA. In order to prevent clipping of the audio signal, the supply voltage must change fast enough to track audio signals. In switched-capacitor based charge pump designs, VPOS and VNEG move by charge sharing which leads to a sharp initial step—in the range of a microsecond—on VPOS and VNEG during gain switching. This can cause an ESD clamp connected between VSSA and VNEG to turn on momentarily and leak. The amount of leakage depends on the ESD clamp design.

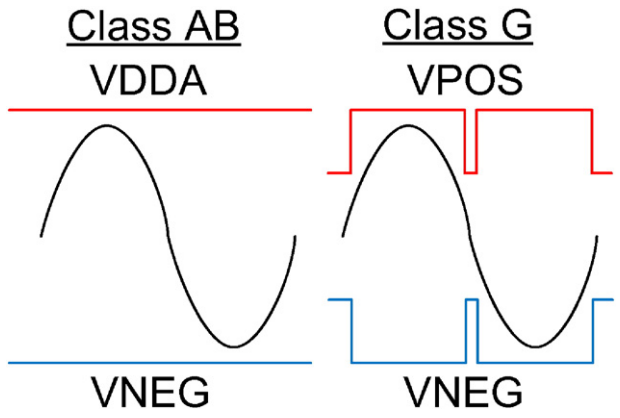

Fig. 2. Class AB and Class G power amplifier supply waveforms.

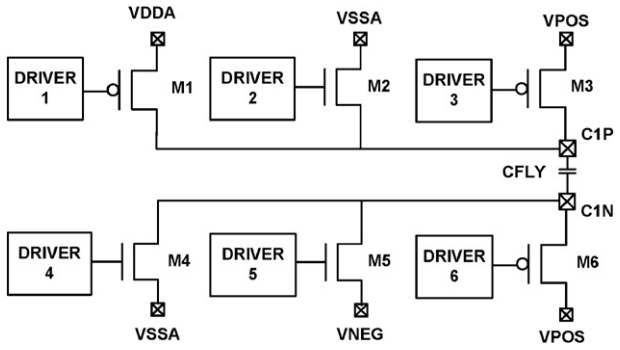

Fig. 3. Switched-capacitor based charge pump design.

4. New HBM ESD protection scheme

A new design has been implemented in 65 nm CMOS technology node. The rough design metric for current handling of an ESD clamp in MOS Conduction mode is 2 mA/μm in this technology. The charge pump switches are around 10 mm in size, which can easily handle a 2 kV HBM level ESD discharges in the MOSFET mode. The modified ESD scheme is shown in Fig. 6. Switches M4 and M5 act as MOSFET mode ESD clamps [2] to replace the ESD clamp connected between VSSA and VNEG in Fig. 5. A diode D7 is connected from VNEG to VSSA to make the clamp bidirectional.

The scheme provides robust ESD protection to limit the pad voltage to a level below the snap-back holding voltage of the parasitic BJT in the switch MOSFETs. For positive discharge between VSSA and C1N, the edetvss signal goes high to turn on the M4 switch, which acts as an ESD clamp; we will call this the M4 clamp. For negative discharge between the same pins, diode D5 and the clamp between VDDA and VSSA provide a discharge path. Similarly, for positive discharge between C1N and VNEG, the edetvdd signal goes high to turn on the M5 switch, which acts as an ESD clamp; we will call this the M5 clamp. Negative discharge between C1N and VNEG is covered by diode D6. Last, for positive discharge between VSSA and VNEG, both the edetvdd and edetvss signals go high to turn on both the M4 and M5 switches together; we will call this the M4M5 clamp.

The entire positive sections are already well protected using the standard ESD protection scheme. The use of internal CP switches as ESD clamp cuts down the area of one ESD clamp and makes the design less sensitive to supply bus resistance, which can be optimized separately for circuit operation.

5. Design of trigger circuit

There are two different trigger circuits for M4 and M5 clamps. These trigger circuits are connected to the closest possible pad to sense the ESD zap with the minimum possible delay. The M4 clamp trigger circuit,

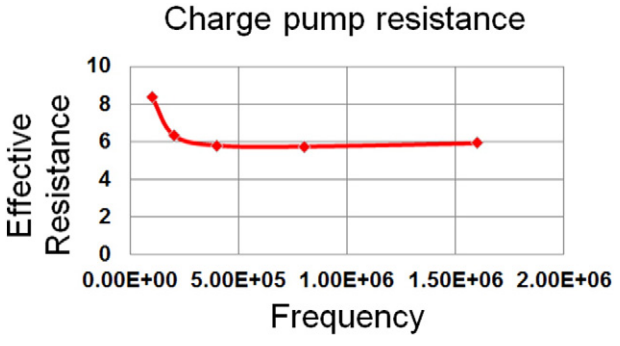

Fig. 4. NCP on-resistance vs. frequency.