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Improved interfacial quality of GaAs metal-oxide-semiconductor device with NH_3-plasma treated yittrium-oxynitride as interfacial passivation layer

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ABSTRACT

The interfacial and electrical properties of GaAs metal-oxide-semiconductor capacitors with yittrium-oxynitride interfacial passivation layer treated by N_2 —/NH_3-plasma are investigated, showing that lower interface-state density (1.24×10^{12} cm^{-2} eV^{-1} near midgap), smaller gate leakage current density (1.34×10^{-5} A/cm^2 at V_{fb} + 1 V), smaller capacitance equivalent thickness (1.43 nm), and larger equivalent dielectric constant (24.5) can be achieved for the sample with NH_3-plasma treatment than the samples with N_2 —/no-plasma treatment. The mechanisms lie in the fact that NH_3-plasma can provide not only N atoms, but H atoms and NH radicals to effectively passivate the high-k/GaAs interface, thus less pinning the Femi level at high-k/GaAs interface.

1. Introduction

Recently, GaAs-based metal-oxide-semiconductor field-effect transistor (MOSFET) with high-k gate dielectric has received increasing attention due to its higher carrier mobility, larger energy bandgap and lower power consumption as compared to those of Si-based MOSFET [1,2]. However, the interface of high-k/GaAs usually has poor quality and a higher interface-state density than the SiO_2/Si interface, thus leading to the Fermi-level pinning [3,4]. So using an interfacial passivation layer (IPL), e.g. Si [5], Ge [6], Al_2O_3 [7], and $Ga_2O_3(Gd_2O_3)$ [8], is very crucial to passivate the interface of high-k/GaAs. However, Si and Ge are amphoteric dopants for GaAs, which may alter the doping concentration or even induce the counter doping of the GaAs substrate, causing the instability of the threshold voltage [9], the low *k* value (~8) of Al_2O_3 limits further device scaling and $(Ga_2O_3)Gd_2O_3$ has been found to be degraded due to absorption of moisture (H_2O) when exposed to air [10].

Yttrium oxide (Y_2O_3) is a very promising dielectric material because of a moderate *k* value (~16), relatively large band gap (5.8 eV) and high thermodynamic stability [11,12] and has been successfully used in MOS devices as high-k gate dielectric on Si [13], Ge [12] and GaAs [11,14] or as IPL on Ge [15,16]. However, pure Y_2O_3 is easy to convert from amorphous to polycrystalline microstructure during the post-deposition annealing, leading to high defect density and unendurable leakage current [17]. Fortunately, nitrogen incorporation into Y_2O_3 can successfully increase the crystalline temperature and occupy the substitutional site of O atom or vacancy in the film to reduce the defect density [17]. Also, incorporation of proper amount of nitrogen in high-k dielectric can increase the k value; reduce gate leakage current; decrease oxygen vacancies; and form strong N-related bonds at/near the dielectric/semiconductor interface to further enhance the thermal stability and reliability of the devices [18–23]. So in this work, YON, which was rarely investigated so far, will be used as IPL for GaAs MOS capacitor with ZrON as high-k dielectric in order to get excellent interfacial and electrical properties. On the other hand, plasma treatment, e.g. N_2-plasma [24,25] and NH_3-plasma [26–28] treatments, directly on the semiconductor surface could efficiently remove volatile elements (e.g. As) and reduce weak Ga—O and As—O bonds, but the N_2 plasma treatment induces damage on the GaAs surface to produce traps, leading to Fermi-level pinning and degradation of current–voltage characteristics [25–29]. This problem is expected to get suppressed by doing the plasma treatment on the IPL, which has received little attention so far. In view of this, the relevant investigation is carried out in this work by using the N_2- or NH_3-plasma treatment on YON IPL before the high-k dielectric deposition. It is expected that an enhanced N incorporation and a better YON/GaAs interface quality could be obtained as compared to its counterpart without plasma treatment on the IPL.

2. Experimental procedure

GaAs MOS capacitors were fabricated on the Si-doped n-type GaAs (100) wafers with a doping concentration of 6×10^{17} cm^{-3}. Firstly, the wafers were cleaned sequentially in deionized water, acetone,

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alcohol and isopropanol respectively for 5 min. Then the wafers were rinsed with deionized water for several times, followed by immersing in HCl solution for 5 min to remove the native oxide and subsequently in 8% $(NH_4)_2S$ for 40 min to sulfur-passivate the surface of the wafers. After drying by N_2, a 2-nm YN was deposited on the GaAs surface as IPL by reactive RF-sputtering of Y target (RF power of 54 W) in an Ar/N_2 (15 sccm/6 sccm) ambient at room temperature and an operating pressure of 0.8 Pa. Then, these samples were divided into three groups: two groups received a plasma treatment in N_2 and NH_3 respectively (denoted as N_2 and NH_3 samples) at a gas flow rate of 4 sccm, 350 °C and a RF power of 120 W; another group without plasma treatment was used as control sample. Subsequently, all the samples were transferred to a sputtering chamber to deposit 7-nm of ZrN by reactive RF-sputtering of Zr target under the same sputtering conditions as YN. Post-deposition annealing of the samples was performed at 600 °C for 60 s in N_2 (500 sccm) + O_2 (50 sccm) to transform YN and ZrN to YON and ZrON, respectively. Finally, Al was thermally evaporated and patterned by photolithography as gate electrode with an area of 7.85×10^{-5} cm^2 and also as the back electrode, followed by N_2 annealing at 300 °C for 20 min to reduce their contact resistance.

High-frequency (HF, 1-MHz) capacitance–voltage (C–V) curve and gate leakage current density vs. gate voltage (Jg–Vg) curves of the samples were measured using HP4284A precision LCR meter and HP4156A semiconductor parameter analyzer, respectively. The chemical states at/near the high-k dielectric/GaAs interface were analyzed by X-ray photoelectron spectroscopy (XPS). Physical thickness of the gate dielectric was measured by ellipsometry. All electrical measurements were carried out under a light-tight and electrically-shielded condition at room temperature.

3. Result and discussion

Fig. 1 shows the HF (1 MHz) C–V curves of the three samples. Obviously, the control sample exhibits poor C–V behavior with largest "stretch-out" and smallest slope in the depletion regime, indicating pinning of Fermi level and a high density of interface states due to weak As—O, As—As, and Ga—O bonds at the GaAs/YON interface [30–33]. However, improved C–V behaviors with less "stretch-out", clear accumulation region and steep slope in the depletion regime are demonstrated for the two plasma-treated samples, especially for the NH_3-treated sample, indicating less interface states and Femi-level pinning effects at the high-k/GaAs interface [6,30,34]. This can be attributed to the fact that the N_2- or NH_3-plasma treatment can reduce the weak As—O, As—As, and Ga—O bonds at the GaAs/YON interface by forming strong N-related bonds, as confirmed by the XPS results below.

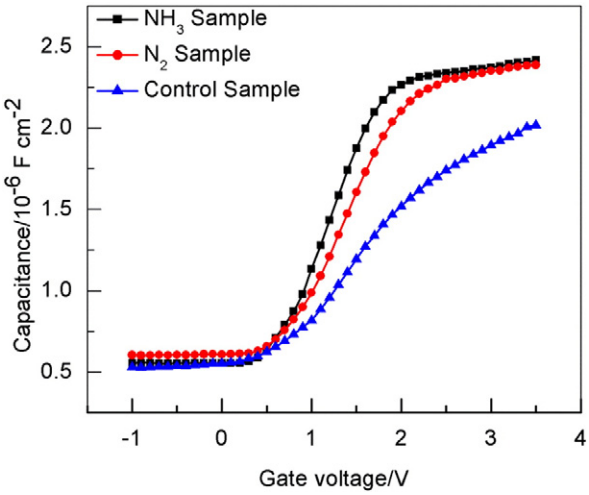

Fig. 1. HF (1-MHz) C–V curve of GaAs MOS capacitors for NH_3, N_2 and control samples.

Table 1
Parameters of the GaAs MOS capacitors extracted from HF C–V curves.

Sample	V_{fb} (V)	D_{it} (/cm^2 eV)	C_{ox} (μF/cm^2)	k	CET(nm)
NH_3 sample	0.98	1.24×10^{12}	2.41	24.5	1.43
N_2 sample	1.11	4.01×10^{12}	2.39	24.2	1.45
Control sample	1.28	1.04×10^{13}	2.02	20.5	1.71

As shown in Table 1, some electrical and physical parameters of the devices are extracted from their HF C–V curves, e.g. flatband voltage (V_{fb}), gate-oxide capacitance (C_{ox}), equivalent k value of the gate dielectric ($k = C_{ox} \cdot T_{ox}/\varepsilon_0$; T_{ox} is the total thickness of the gate dielectric; ε_0 is the vacuum permittivity), capacitance equivalent thickness ($CET = \varepsilon_0 k_{SiO2}/C_{ox}$, where k_{SiO2} is relative permittivity of SiO_2), and interface-state density (D_{it}) near the midgap determined by the Terman's method [35]. The positive shift of V_{fb} indicates the existence of negative charges in the dielectric film and at/near the interface [36], which are probably associated with acceptor-like interface states and near-interface electron traps. Obviously, the NH_3 sample has the smallest V_{fb} (0.98 V), followed by the N_2 sample (1.11 V) and the control sample (1.28 V). This is likely due to the fact that the N_2- or NH_3-plasma treatment on YN IPL is able to incorporate more nitrogen atoms in the IPL for filling the oxygen vacancies produced during the subsequent post-deposition annealing [19,30,36] so that the out-diffusions of Ga and As atoms from the substrate to the high-k dielectric can be better blocked by the plasma-treated YON IPL [18], especially for the NH_3-plasma treatment (since NH_3 has a lower ionization energy to produce N^+ ions [19] than N_2, more nitrogen atoms can be incorporated in the IPL during the NH_3-plasma treatment). Furthermore, the NH_3 sample exhibits larger C_{ox} and equivalent k value, and smaller CET than the N_2 and control samples, further indicating that the NH_3-plasma treatment can more effectively suppress the formation of low-k interfacial oxide on the GaAs surface [18,27] due to more nitrogen incorporation near the YON/GaAs interface for the former than the latter. In addition, lower D_{it} is observed for the two plasma-treated samples (1.24×10^{12} cm^{-2} eV^{-1} for NH_3 sample and 4.01×10^{12} cm^{-2} eV^{-1} for N_2 sample) than the control sample (1.04×10^{13} cm^{-2} eV^{-1}), indicating that the NH_3- and N_2-plasma treatments can effectively reduce the defects at the interface, especially the former, and the involved mechanisms are analyzed below.

The gate leakage characteristics of three GaAs MOS capacitors are shown in Fig. 2. A much larger J_g is observed for the control sample than that of the NH_3 and N_2 samples, with the smallest for the NH_3 sample, e.g. 1.34×10^{-5} A/cm^2, 3.48×10^{-5} A/cm^2 and 4.83×10^{-4} A/cm^2 at V_{fb} + 1 V for the NH_3, N_2 and control samples, respectively. The interface-trap-assisted tunneling is suggested to be the main reason for the larger gate leakage current [2,6] because there are more interface

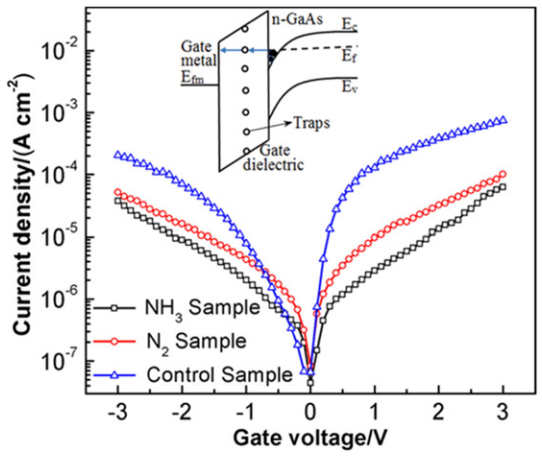

Fig. 2. J_g vs.V_g characteristics of GaAs MOS capacitors. The inset is the schematic diagram of trap-assisted tunneling in gate dielectric.