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Temperature dependence of the electrical characteristics up to 370 K of amorphous In-Ga-ZnO thin film transistors

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ABSTRACT

The temperature dependence in the typical temperature operating range from 300 K up to 370 K of the electrical characteristics of IGZO TFTs fabricated at temperatures not exceeding 200 °C is presented and modeled.
It is seen that up to $T = 330$ K, the transfer curves show a parallel shift toward more negative voltages. In both subthreshold and above threshold regimes, the drain current shows Arrhenius-type dependence. In the latter case, for low temperatures, the activation energy is around 0.35 eV for $V_{GS} = 10$ V, reducing as V_{GS} is increased. The observed behavior is consistent with having the VRH transport mechanism as the predominant one in conduction.

1. Introduction

Amorphous oxide semiconductor thin film transistors (AOSTFTs) have been dedicated much research work due to their advantages with respect to other types of thin film transistors, TFTs, such as high optical transparency, relatively high electron mobility, as well as low temperature and relatively low cost processing techniques [1–4]. Although the first ZnO TFTs were reported as early as in the 1960s, [5], relatively high mobility and low temperature processing were achieved much later [6].

To increase carrier mobility and device stability, amorphous multi-component oxides have been studied, where several binary oxide components such as Ga_2O_3, In_2O_3 and HfO_2 are added to the ZnO as base semiconductor. The most successful multi-component oxides are Indium–Gallium–Zinc oxide, (IGZO) and Hafnium–Indium–Zinc oxide, (HIZO). The use of these multi-component oxides has provided a significant reduction in both the bias and light-stress instability [7–9].

In order to understand and describe the properties of the materials, several works can be found, in which the electrical characteristics are analyzed at temperatures below 273 K to determine the conduction mechanisms in AOSTFTs [10–15]. However, results are not conclusive yet, because although several possible mechanisms have been identified, the predominant mechanism will always depend on the specific conditions of the device fabrication processes.

Due to self-heating or to circuit operation conditions, AOSTFTs used in flat panel displays have to work in the temperature range between 243 K and 360 K, according to the temperature specifications of commercial displays. At this temperature range, however, the AOSTFTs can degrade [16,17]. For this reason, the variation with temperature of their electrical characteristics in the temperature range up to 370 K is also an important piece of information to consider for different applications and should be included in models used for circuit design. In this work we first analyze the temperature dependence up to 370 K of the electrical characteristics of IGZO TFTs fabricated with temperatures processes not exceeding 200 °C, to determine the transport mechanisms present in the devices and to obtain the temperature coefficients of V_T and V_{FB} to be used for modeling their electrical characteristics with temperature. The observed temperature dependence can be well represented, after incorporating the temperature dependence of the model parameters to an AOSTFT model previously developed by our group.

2. Experimental part

The IGZO TFTs were fabricated using a bottom-gate top contacts configuration, as shown in Fig. 1a. For this process, gate metal is patterned on 100 nm of Au deposited on top of 10 nm of Cr (adhesion layer). Both metals were deposited in situ by electron beam. Next, 90 nm of HfO_2 gate dielectric is deposited at 100 °C by atomic layer deposition, followed by 70 nm of IGZO layer, obtained by pulsed laser deposition (PLD) at 20 mTorr oxygen pressure. Immediately after IGZO deposition, devices were annealed in O_2 at 200 °C for 1 h. The sample is subsequently covered by 500-nm of poly-p-xylylene-C (Parylene-C) protective/

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Table I
Extracted model parameters at T = 300 K.

T [K]	V_T [V]	V_{FB} [V]	μ_{FETo} [cm^2/Vs]	μ_{FET} [cm^2/Vs]	To [K]	g_{deep} [cm^{-3}]	γ	γ_b	α_s	m	λ	R [Ω]
300	3.6	2	1.7	7.1	830	8.5×10^{19}	0.6	3.6	0.46	2.27	0	436

hard-mask film deposited by chemical vapor deposition (CVD) at room temperature at 1 mTorr. Gate dielectric vias were opened using photolithographic process and wet etching for the HfO_2. Source-Drain (*S-D*) vias were opened through the hard-mask, using O_2 RIE. Then, 100 nm of Al were deposited by electron beam and patterned to form the *S-D* contacts. Finally, devices were annealed at 100 °C in N_2 for 1 h. Fig. 1b shows an optical micrograph of a typical device. TFTs with different channel widths ($W = 40$, 80 and 160 μm) and channel length ($L =$ 20, 40 and 80 μm) are included on each die.

Electrical measurements were done in dark, at different temperatures and in vacuum conditions. We used a K20 programmable Temperature Controller and measurement chamber from MMR Technologies Inc. and a Keithley 4200 semiconductor characterization system.

The linear transfer curves and the output characteristics of devices were measured in the temperature range between 300 K and 370 K, which corresponds to a typical operating temperature range. Subsequent measurement cycles were done in order to guarantee that the variation of the drain current was due to the temperature variation and not to instability effects. Since the characteristics for all devices showed a similar behavior, results will be shown for devices with $W = 80$ μm and $L = 40$ μm.

3. Analysis and discussion of results

Fig. 2a and 2b show the experimental data of the linear transfer curve in semilog and linear plot and Fig. 2c show the output characteristics, at room temperature, respectively.

The measurements performed at room temperature were used to determine the set of basic device parameters shown in Table 1. The extraction procedure is described in [18]. Modeled characteristics are also included in Fig. 2 to demonstrate the good agreement between measured and modeled characteristics.

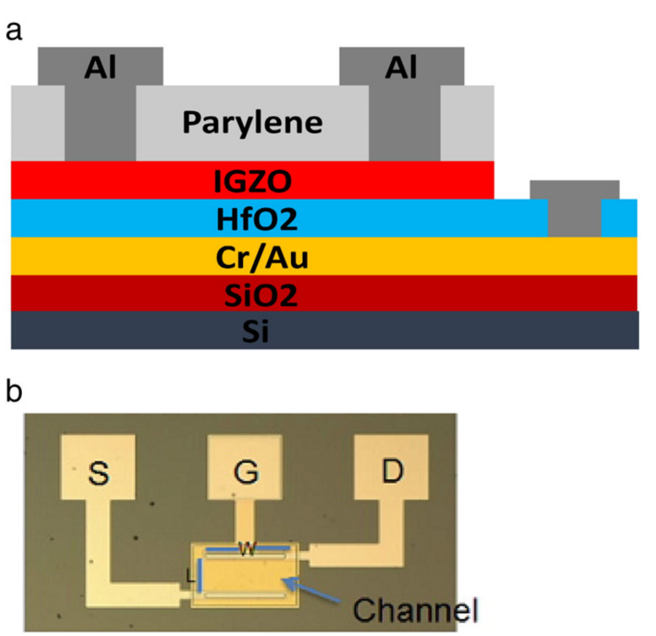

Fig. 1. (a) Cross section and (b) photo of the device structure.

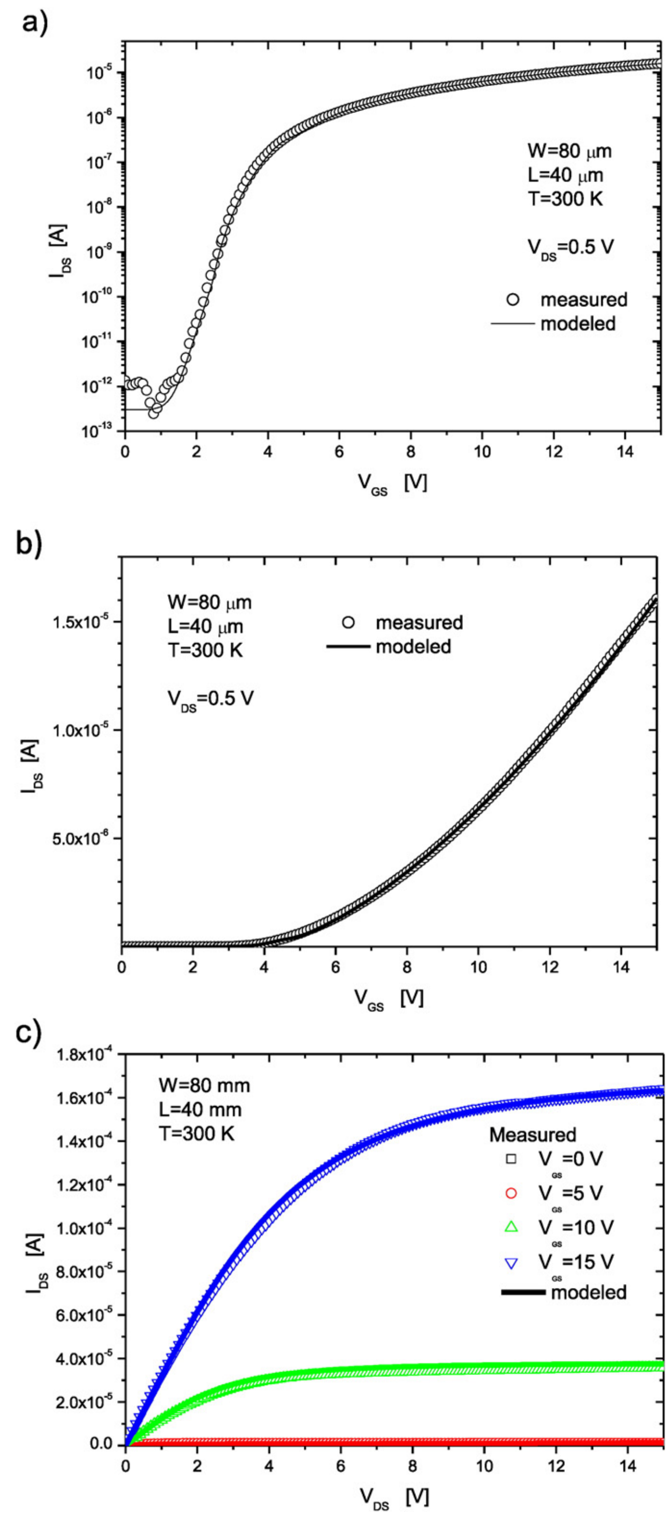

Fig. 2. Measured at 300 K and modeled a) and b) transfer characteristics in semilog and linear plot, respectively; c) output characteristics.