Microelectronics Reliability 56 (2016) 121–128

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Failure of electrical vias manufactured in thick-film technology when loaded with short high current pulses

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ARTICLE INFO

Article history:
Received 28 June 2015
Received in revised form 6 October 2015
Accepted 7 October 2015
Available online 12 December 2015

Keywords:
Thick-film hybrid technology
Screen-printing
Via
Interconnect
Failure
Ampacity
Silver-palladium
Finite element method (FEM)

ABSTRACT

The high-current failure of electrical interconnects (through-metalized vias) manufactured in thick-film technology is investigated. A large number of vias were measured in a four-wire-setup by applying short time high-current pulses. The experimental conditions ensured that approximately half of the tested vias were destroyed during the tests. The high-current failure mechanism was identified to be a kind of a self-accelerating melting process. It was also implemented in a "Finite Element Method" (FEM)-model. The FEM-model delivered not only the time-dependent voltage drops over the through holes (which is proportional to the through hole resistance), but also the time-dependent temperature, conductivity, and current density distributions inside of the vias during current load. Input parameters for the model were material properties and sample geometries. Analyzed cross-section micrographs of destroyed vias and the temperature maxima received from the FEM-model agreed well. Furthermore, measured and modeled voltage drops during failure were compared and agreed also very well.

1. Introduction

Built-in control units are widely used in the field of automotive and other electronic devices and systems with a rapidly increasing trend [1,2]. Thick-film hybrid technology is used extensively especially to produce electronic circuits for the use in harsh environments [3–5] like engine control units or transmission control units. The advantages of this robust technology are also utilized for the production of several types of sensors that are used in harsh environments like automotive exhaust [6–9]. Typical thick-film hybrid circuits consist of two parts, the thick-film substrates and discrete components. The thick-film components are produced from thick-film materials by screen-printing on alumina substrates, followed by drying and firing at peak temperatures of about 850 °C under oxidizing furnace atmospheres [10]. Typical thick-film components are conductors (interconnection lines, terminals and pads), resistors, dielectric layers and overglaze protection layers. The discrete surface mounted devices are integrated onto the thick-film substrate by different processes like gluing, soldering, die-bonding and wire-bonding. The materials and the processes of both, mounting of discrete components [11,12] and the thick-film part [13–27] have been studied intensively in the past. Vias used in adjacent fields to thick film technology have also been studied persistently during recent years, like low temperature co-fired ceramics (LTCC) [30,31] and printed circuit boards (PCB) [32].

In order to establish an electrical connection between top and bottom layer of the ceramic substrates, electrical vias are used [28,29]. Such vias are made by laser-drilling of holes through the ceramic substrates that are then partly filled or plated with a conductor. Fig. 1a shows a top view and Fig. 1b shows a micrograph of a typical via for low ampacity.

The same screen-printing process as mentioned above is also used to manufacture the vias. During printing, the substrate is sucked in the printing nest in order to draw the paste into the through holes. This produces an approximately 20 μm thick metallization, which covers the outer surface. This step (print-dry-fire) is carried out once again from the rear side to cover the lateral surface of the vias. After firing, a few micron thick metallization layer remains on the surface.

The application conditions vary from low-power stationary operation on low pulse currents to higher pulse currents. The different operation of the vias results in different failure mechanisms. Stationary operation of the vias at very low amperage leads to a uniform heating of the entire substrate. With higher currents, a more spontaneous failure of the vias occurs. Local higher current densities lead to locally higher heat generation. The generated heat cannot diffuse fast enough from the metallization layer to the substrate (heat sink). This leads to a very strong and rapid temperature increase, causing the vias to fail as described in this paper. When looking at extremely high current pulses for a very short time, more failure mechanisms have to be considered, since the electric field leads to destruction the vias. The scope in this

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http://dx.doi.org/10.1016/j.microrel.2015.10.011
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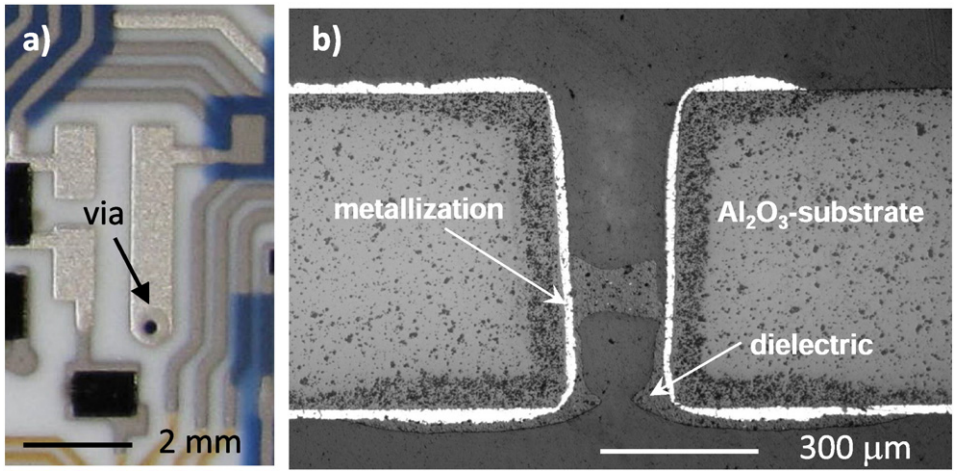

Fig. 1. a) Top view of an exemplary via in thick-film hybrid technology. b) Transverse section micrograph of a conventional thick-film via. The metallization layer appears in white.

paper is on current pulses up to 30 A for a duration of 100 ms. In earlier work, we have studied the behavior of those conventional vias with respect to the processes occurring at pulsed current load [33], especially the temperature increases as a consequence of ohmic losses were studied. The generated heat Q is proportional to the square of the current I, according to Eq. (1).

$$Q \propto I^2 \tag{1}$$

Conventional vias are already very reliable for small currents, but in order to expand their application to higher currents, it is important to obtain insights in the thermal processes that occur when high currents are impressed into the vias. In order to analyze the resistance over time as a result of short time constant current pulses, vias were tested at current pulses between 2 A and 30 A. Furthermore, an FEM-model was developed, which confirmed and explained the experimental data. With this model the influence of different input parameters like via geometry and via material parameters on the resulting temperatures were investigated. Beneath the time-dependent voltage drops, the resulting via resistances and ohmic losses, also the timely and locally resolved temperature, conductivity and current density distribution in the metallization layer of the vias were obtained. The current I defines the inward current density J.

$$J = \frac{I}{A} = \frac{I}{2\pi \cdot r_{\text{outer}} \cdot t_{\text{r}}}, \tag{2}$$

where r_{outer} is the radius of the reinforcement ring on top of the substrate and t_{r} depicts the thickness of the reinforcement ring, as can be seen in Fig. 2. In reality, many vias are connected to the circuit by conductor tracks. In this work, the reinforcement ring was chosen deliberately to ensure to investigate the influence of the vias itself and not the manner they are connected to the surrounding. That fact was also considered in the conduction of the measurements described further below, as the measured vias were surrounded by metallization pads. At the edge of the reinforcement ring on the bottom of the substrate, the electrical potential φ was set to zero. The meaning of the geometrical variables is depicted in Fig. 2. The temperature distribution at the end of a current pulse is also plotted in Fig. 2. A point of maximum temperature occurs, which will be called hot spot in this article.

In the present work, the failure of vias during short time high current pulses shall be implemented in the model and compared with data obtained from a large test series of 1890 vias.

2. Measurement setup

All measured samples were taken directly from the series production of a transmission control unit. They were taken from seven different lots with a total number of 1890 tested vias according to Table 1.

The measurements were accomplished in four-wire-technique in order to apply a constant current pulse and simultaneously measure the transient voltage drop.

A holding fixture using needle springs was used to contact the vias in order to firmly clamp the needles on the contact pads and to ensure low contact resistances. Then, constant current pulses were applied. Each pulse lasted 100 ms and between two consecutive pulses a pause of 10 s allowed the sample to cool down to room temperature again. Each via was measured at gradually increased currents from $I = 2$ A up to 30 A. The current was generated using a current power source (Delta Elektronika SM52-AR60 Power Supply) and a current sink (Höcherl & Hackl PL506 Electronic Load). Simultaneously, the voltage drop over the vias was recorded by a digital oscilloscope (Tektronix

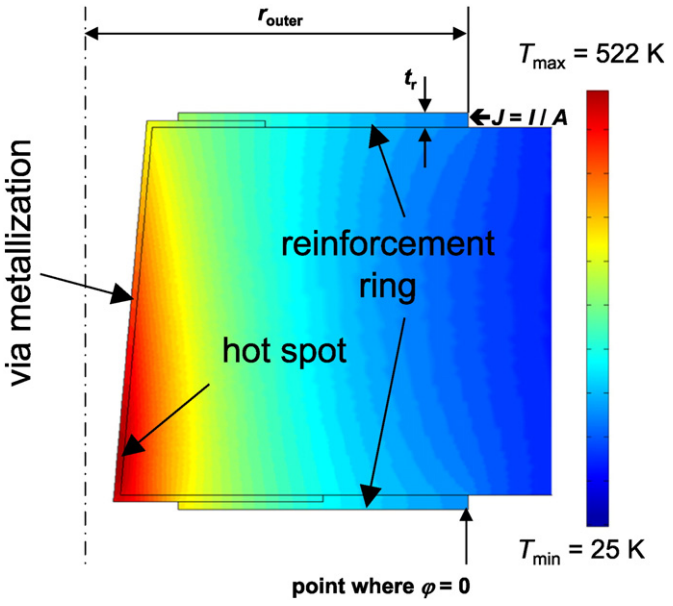

Fig. 2. A sectional view of the temperature distribution obtained from the FEM-model. The current is a result of the inward current density J on the edge of the reinforcement ring on top of the substrate, while setting the potential φ to zero at the edge of the reinforcement ring on the bottom of the substrate. The point of highest temperature (hot spot) occurs near the drilling outlet.