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Introductory Invited Paper

Ultra-thin dielectric breakdown in devices and circuits: A brief review

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ABSTRACT

Time-dependent dielectric breakdown (TDDB), in which the traps in oxide bulk form a conducting path under application of stress voltage for long period of time, has emerged as one of the important sources of performance degradation in advanced devices. In this paper, we give an overview of the recent progress in the understanding of ultra-thin dielectric breakdown in devices and consider its impact at the circuit-level. From the device point of view, the breakdown (BD) phenomenon, including the BD statistics, trap generation models, and BD evolution in ultra-thin dielectric are presented followed by the recent studies on TDDB in high-*k* metal gate (HKMG) devices and magnetic tunnel junction (MTJ) memories. On the circuit side, we explore methodologies for circuit lifetime assessment, the impact of TDDB on circuit performance degradation, and design techniques to improve circuit reliability.

1. Introduction

Aggressive scaling of device dimensions and supply voltage to achieve higher integration density and lower power operations require ultra-thin gate oxides for maintaining gate-controllability and drivability. However, the ultra-thin oxides not only lead to increased gate leakage current but also make devices susceptible to time-dependent dielectric breakdown (TDDB). This is due to the fact that the number of defects (=traps) required for breakdown (BD) in ultra-thin oxides is smaller than that in thicker oxides. When the stress voltage is applied, the insulating properties of the oxide degrades in mainly two stages: (1) oxide degradation, called wear-out phase of oxide and (2) oxide BD. At the beginning, in the wear-out phase, the generated traps slowly increase the stress induced leakage current (SILC) as shown in Fig. 1(a). With the continuous increase in the stress time, the gate leakage current becomes noisy after a soft BD (SBD) and finally experiences a sudden jump after a hard BD (HBD). Further, it has been shown that the I–V characteristics of the dielectric after a SBD can be described by a power law while the conduction after a HBD becomes ohmic, as illustrated in Fig. 1(b).

Since the occurrence of the BD is related to randomly generated defects in the oxide, reliability evaluation requires a thorough understanding of the defect generation process and a physics-based model for BD statistics to evaluate its impact on circuits. Although, in recent studies, BD statistics has been successfully predicted by percolation theory [1–6], the exact defect generation mechanism is still under debate. In addition, since the gate leakage due to BD (I_{G_BD}) in ultra-thin oxide is few orders of magnitude smaller than that in thicker oxide, the first BD event in thin oxides might not cause failure of device. As a result, significant research efforts in recent years have been devoted to understanding post-BD phenomenon, such as SBD, progressive BD (PBD), and HBD [7–9].

On the other hand, the emergence of advanced devices, such as high-*k* metal gate (HKMG) transistors and magnetic tunnel junctions (MTJ) [10–15], has added new dimensions to TDDB study [15–25]. For example, BD statistics of HKMG device is found to be different from conventional SiO_2 devices due to the stack oxide structure. With understanding of statistics and physics of BD at the device level, the impact of TDDB on circuit performance can be evaluated. Note, the reliabilities of various circuits, such as ring oscillator (RO) and static random-access memory (SRAM) have been evaluated by circuit-level reliability tests and compact models [1,2,26–32]. However, most compact models consider the first breakdown. Hence, more research effort is required to implement the post-BD phenomenon in compact models for better prediction of circuit reliability.

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The rest of the paper is organized as follows: Section 2 presents the observations of TDDB in both conventional and emerging devices. This section includes sub-sections on the percolation theory, voltage dependence of defect generation and BD evolution, including SBD, PBD, and HBD. In addition, recent studies on emerging devices, including HKMG devices and MTJ are also reviewed. Section 3 covers the circuit lifetime assessment, TDDB impact on circuits (logic and memory), monitoring circuits to assess TDDB degradation, and circuit design techniques for improving reliability. Finally, Section 4 presents conclusions and summarizes some open problems.

2. Statistics and physics of breakdown

2.1. Statistics and physics of breakdown for conventional SiO_2 devices

Standard reliability assessment methodology is based on the statistics of breakdown (BD) time and the physics of defect generation (i.e. the dependence of defect generation on stress conditions). In this subsection, the percolation model to predict BD statistics is first presented, followed by a brief review of three physics-based defect generation models and their voltage dependences. In addition, we discuss recent studies on BD evolution, such as soft BD (SBD), progressive (PBD), and hard BD (HBD). Since the first BD might not cause failure in ultra-thin oxide devices, the oxide degradation after the first BD needs to be well understood in order to better evaluate oxide reliability.

2.1.1. Percolation model

The first statistical TDDB model for the distribution of BD time has been proposed by Suñé et al. [33]. In this model, generated defects are assumed to be randomly distributed in the oxide using Poisson statistics. In addition, BD time is defined as the time when the generated defect density reaches a critical defect density (D_{BD}). While this model successfully predicts the important features of BD statistics, such as single slope in the Weibull plot and area independence of the Weibull slope [34], it is not capable of characterizing the dependence of D_{BD} and the Weibull slope on dielectric thickness (t_{ox}). In order to successfully address this issue, a new model using percolation theory is proposed by Degraeve in [3].

In the percolation model [3] as illustrated in Fig. 2, BD time is defined as the time when defects in the oxide connect the gate to the channel, instead of adopting the critical defect density from [33]. This model concludes that thin oxides require fewer defects to create a percolation path than thick oxides. This leads to a larger spread of BD time and a smaller Weibull slope in thinner oxides. Following Poisson statistics, the simulation results of this model

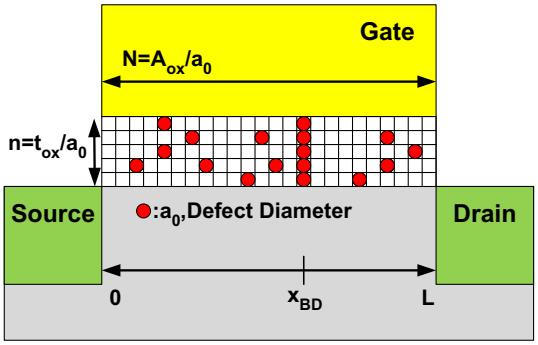

Fig. 2. Device level cross section with a percolation path.

have demonstrated a decrease in the Weibull slope with thinner oxides and a relationship between the hole fluence (Q_{tot}) and defect generation as given by (1):

$$D_{tot} = kQ_{tot}^{0.56} \tag{1}$$

where D_{tot} is the trap density and k is a constant and $Q_{tot} = Jt$, where J is the tunneling current density. The defective probability for each cell (F_{cell}) in the oxide can be defined as [1,2]. In this model, the total area of dielectric, A_{OX} is divided into small cells (a_0) of the area shown in Fig. 2:

$$F_{cell} = ct^{0.56} \tag{2}$$

where c is a constant. The probability of a defective path (F_{path}) in the oxide can be expressed as:

$$F_{path} = 1 - F_{no\text{-}path} = 1 - \left(1 - F_{cell}^{n}\right)^{N} \tag{3}$$

where $n = t_{ox}/a_0$ and $N = A_{OX}/a_0$ in Fig. 2. From (3), the Weibit for BD time in the Weibull plot can be expressed as:

$$W_{BD} = \ln\left[-ln(1 - F_{path})\right] = ln(N) + nln(c) + 0.56\ nln(t) \tag{4}$$

Consequently, the dependence of the Weibull slope (β) on oxide thickness can be obtained from the third term in (4) which is same as t_{ox}/a_0. Furthermore, recent reports have found the dependence of stress voltage on the Weibull slope [5,6]. Although the physics behind the voltage dependence is not yet clear, it has been observed that the Weibull slope increases with gate voltage. In [5,6], the authors demonstrate that the voltage dependence becomes stronger in thicker oxides.

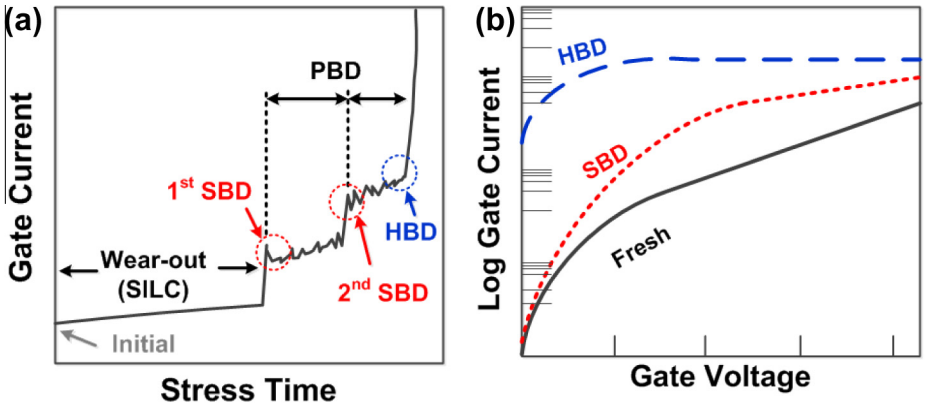

Fig. 1. (a) A typical behavior of gate leakage current with an increase in stress time and (b) typical I–V characteristics during stress.