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Improved performance of nanoscale junctionless transistor based on gate engineering approach

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ABSTRACT

In this paper, we propose an effective method to improve the electrical characteristics of dual-material-gate (DMG) junctionless transistor (JLT) based on gate engineering approach, with the example of n-type double gate (DG) JLT with total channel length down to 30 nm. The characteristics are demonstrated and compared with conventional DMG DGJLT and single-material gate (SMG) DGJLT. The results show that the novel DMG DGJLT presents superior subthreshold swing (SS), drain-induced barrier lowering (DIBL), transconductance (G_m), ON/OFF current ratio, and intrinsic delay (τ). Moreover, these unique features can be controlled by engineering the length and workfunction of the gate material. In addition, the sensitivities of the novel DMG device with respect to structural parameters are investigated.

1. Introduction

The conventional metal–oxide–semiconductor field-effect transistors (MOSFETs) impose challenges, such as enlarged gate leakage and added serious short-channel effects (SCEs) with the continuous miniaturization of device sizes at nanoscale regime. Multiple gate FETs have better scalability due to its superior controllability of the gates on the channel region. However, very abrupt source and drain junctions requirement put challenges in doping profile techniques and thermal budget. As an alternative, junctionless transistors (JLTs) with a uniform doping concentration and type throughout the channel and source/drain extensions are fabricated to overcome these challenges. Their electrical characteristics and temperature dependence have been studied [1–5], and it has been demonstrated that JLTs have extremely low leakage currents and simple fabrication processes and are less susceptible to SCEs when compared with classical inversion-mode devices [1,2,5,6]. However, the high doping concentration in the channel region reduces carrier mobility, which hurts drive current and transconductance of JLTs [2,6–8].

At the same time, dual-material gate (DMG) devices have been theoretically studied [9–16] and fabricated [17–19]. Gate engineering technique such as dual metal gate (DMG) MOSFET has been firstly proposed in which the structure has two gates with different work functions [20]. It has been shown that the DMG structure can offer improved carrier transport efficiency, transconductance and reduced drain-induced barrier lowering (DIBL) compared with single-material gate (SMG) conventional MOSFETs. By adjusting the metal workfunctions, channel potential and electric field distributions along the channel can be controlled [10,11,17]. Long et al. [17] have experimentally shown that DMG MOSFET offers simultaneous improvement of SCE. As the operation principle of JLT is different from conventional MOSFET, it is interesting to see the performance of DMG JLT compared with SMG JLT. Lou et al. [21] have reported that for a JLT, SCE can be improved by incorporating a DMG instead of SMG. While I_{OFF}–off-state current–is the contributor to the stand-by power dissipation in the device, it is equally important that I_{ON}–the on-state current–be high since the drive capability of the transistor is a strong contributor to the speed in a capacitance-dominated environment. Thus, the ratio of the two (I_{ON}/I_{OFF}) is a useful parameter that accounts for both these.

In order to achieve devices with lower SS, higher I_{ON}/I_{OFF} and reduced SCEs at nanoscale regime, we present a method based on gate engineering approach, which includes the change of the physical dimension of the gate for the DMG JLTs with the example of n-type double-gate (DG) MOSFETs. Unlike the conventional DMG structure, in which takes advantage of gate material workfunction difference in such a way that the threshold voltage near the source is more positive than that near the drain, leading to a more rapid acceleration of charge carriers in the channel and a screening effect to suppress SCEs, the novel DMG device consists of three metal gates with two different materials: two side gates, which are located near the source and drain, respectively, and

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one inner gate, which is located between the side gates. The threshold voltage of the novel DMG DGJLT under the side gates is equal and lower than that under the inner gate, so that the side gates turn on before the inner gate does. As a result, the novel DMG device has effectively a longer channel length when it is off and shorter channel length when it is on, and this sharper switch between on-state and off-state improves subthreshold characteristics, and lowers I_{OFF} as well. Based on this gate modulation, the novel DMG DGJLT allows effective control of the effective channel length, an improvement in I_{ON}/I_{OFF} and intrinsic delay, and low power transistors at gate lengths well below 30 nm.

In this paper, we propose a novel DMG DGJLT based on gate engineering approach. Their characteristics are investigated by 2-D Sentaurus TCAD simulations [22]. Key design parameters such as the lengths of inner gate and side gates and the influences of different workfunction configurations are analyzed in later sections.

2. Device structure and simulation

The device structures for a novel n-type DMG DGJLT and a conventional n-type DMG DGJLT with the same channel length L, which is used as a reference for comparison, are shown in Fig. 1. For better illustration, the conventional n-type SMG DGJLT is not shown in figure. An n-type DGJLT has homogeneous (N+) and uniform doping for the source, channel, and drain region. The operation of DGJLT is explained in [23–25]. As we all know, the conventional SMG DGJLT has only one metal gate. However, the conventional DMG DGJLT has two metal gates, M1 and M2, with different workfunctions, denoted by W_{M1} and W_{M2}, respectively, as shown in Fig. 1(a). Recently, Lou et al. [21] have reported that in conventional DMG JLT, out of different combinations of L_{M1} and L_{M2}, $L_{M1}/L = 1/2$ and work-function difference of δW, $\delta W = W_{M1} - W_{M2} = 0.5$ eV give the overall best characteristics of the device. Thus, in this paper, for conventional DMG devices, W_{M1} and W_{M2} are set to be 5.3 eV and 4.8 eV, respectively, which correspond to acceptable threshold voltage for the devices. The values of L_{M1} and L_{M2} are set to be 15 nm, along with the total channel length of 30 nm.

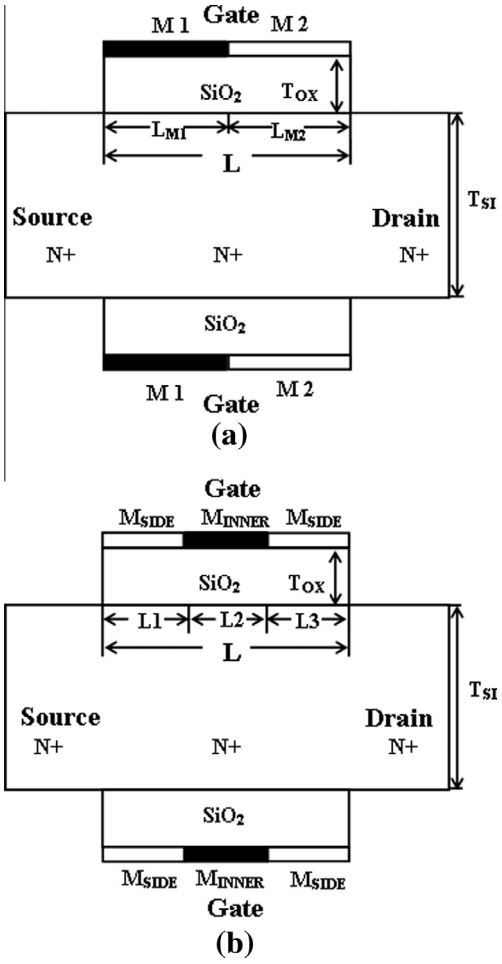

Fig. 1. Cross-sectional view of (a) conventional DMG DGJLT and (b) novel DMG DGJLT.

Fig. 1(b) shows that the gate region of the novel DMG DGJLT is divided into two parts—two side gates (M_{SIDE}) and one inner gate (M_{INNER}). The inner gate's workfunction is denoted by $W1$, and both side gates have the same workfunction, which is denoted by $W2$. Metal, M_{INNER} has higher workfunction than M_{SIDE}, such that threshold voltage of M_{INNER}, $V_T(M_{INNER})$ is greater than $V_T(M_{SIDE})$, in which inner gate can be renamed as a "control gate", while the side gate near the drain is functioning as a "screen gate", respectively. This gate structure implies that channel region underneath the "control gate" becomes the effective channel length, L_{eff}, while the region underneath the "screen gate" acts as drain extension, which is similar to the conventional DMG device. We define $L1$ as channel length for metal M_{SIDE} near the source, $L2$ as channel length for metal M_{INNER}, and $L3$ as channel length for metal M_{SIDE} near the drain. $L = L1 + L2 + L3$ is the total channel length. However, $L1$ acts as "source extension", which is the major difference between the proposed device and the conventional one. The basic idea of the novel DMG device is to separate the source and drain extensions from the active channel of the MOSFET by a gated low threshold voltage region. The gate length ratio of the metal gates and their workfunction difference affect the device characterizes significantly. The values of $L1$, $L2$, and $L3$ are initially set to be 6 nm, 6 nm, and 18 nm, respectively. And the values of $W1$ and $W2$ are assigned to be 5.3 eV and 4.8 eV, respectively. The detailed parameters used for simulations in this paper are summarized in Table 1. All the devices are fully depleted under subthreshold condition. The lengths and workfunctions of the metal gates in the novel DMG device can be varied in the simulations.

Moreover, it is worth mentioning that the novel DMG device has a shorter effective channel length than the conventional counterparts in the on-state, even though the total channel lengths are kept to be same, as shown in Table 2. For fair comparison, we have also simulated the conventional DMG JLT with $L_{M1} = 6$ nm and $L = 30$ nm, in order to make a further discussion of the function of $L1$. All the other parameters are same as shown in Table 1. Fig. 2 shows depletion region contours of the devices at $V_{DS} = 0.05$ V and gate voltage overdrive $V_{GT} = 0.06$ V, and V_{GT} is defined as $V_{GT} = V_{GS} - V_{TH}$, where V_{GS} is the gate voltage and V_{TH} is the threshold voltage. It is observed that the novel DMG device starts to turn on while the conventional one still remains at the off-state. Thus, the switching speed of the proposed DMG DGJLT is faster, which brings various improved performances. In Fig. 3, the electron concentrations of the devices at $V_{DS} = 1.0$ V and $V_{GT} = 0.6$ V are shown. It is observed that the electron concentration of the proposed device in the "source extension" is increased due to the lower workfunction of the side gate above $L1$. As a result, the drive current is further enhanced owing to the more electron injection into the channel region.

Electrical characteristics for the devices are simulated using 2-D SDEVICE simulator with default parameter coefficients [22]. For all simulations, uniform doping concentration throughout the channel and source/drain regions is assumed. The simulation is drift–diffusion based without impact ionization, and the mobility model includes the effects of doping concentration and electric field. The density gradient model applied in [20,26,27] is utilized to account for the quantum effects. Band-gap narrowing (BGN) due