Microelectronics Reliability 55 (2015) 332–336

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Investigation and comparison of analog figures-of-merit for TFET and FinFET considering work-function variation

Ko-Chun Lee, Ming-Long Fan, Pin Su *

Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan

ARTICLE INFO

Article history:
Received 27 July 2014
Received in revised form 15 November 2014
Accepted 15 November 2014
Available online 12 December 2014

Keywords:
TFET
Work-function variation
Analog FOM
Output resistance
Intrinsic gain
Cutoff frequency

ABSTRACT

This paper investigates and compares the impacts of metal-gate work-function variation on important analog figures-of-merit (FOMs) for TFET and FinFET devices using 3-D atomistic TCAD simulations. Our study indicates that, at 0.6 V supply voltage and 0.2 V gate-voltage overdrive, TFET exhibits superior variation immunity regarding transconductance to drain–current ratio (g_m/I_{DS}), output resistance (R_{out}) and intrinsic gain, and comparable variability in g_m and cutoff frequency (f_T) as compared with the FinFET counterparts. In addition, how the correlations between pertinent parameters (e.g., g_m and R_{out}) impact the variation immunity of important analog FOMs are analyzed. Our study may provide insights for low-voltage analog design using TFET/FinFET technologies.

1. Introduction

To maintain high enough I_{ON}/I_{OFF} under low supply voltage, new post-CMOS devices with subthreshold swing below the 60 mV/decade limit of room-temperature MOSFET are important. Using band-to-band tunneling as the major conduction mechanism, Tunnel FET (TFET) [1–4] is a promising device structure that may surmount this physical limit. While currently it is difficult for TFET to reach the required I_{ON} performance for logic applications [2–4], it has been pointed out that TFET can be very attractive for low-power analog applications such as operational transconductance amplifier (OTA) [5–9].

With the scaling of device dimensions, random variability emerges as reliability crucial concern and may hinder the feasibility of TFET [10–12]. The impact of variability on TFET analog characteristics, however, has rarely been known and merits investigation. Among various variation sources, the work-function variation (WFV) [13–16] associated with the metal gate has been suggested as the most important variation source for TFET [3]. Moreover, [13,17] have pointed out that the threshold-voltage (V_{th}) variation can be mitigated by thinner EOT provided by high-k metal-gate except for WFV. In this paper, using 3-D atomistic TCAD simulations [13,18], we investigate the impacts of WFV on important analog figures-of-merit (FOMs) for TFET, and compare our results with the FinFET counterparts.

2. Simulation methodology

To simulate the band-to-band tunneling current for TFET, the non-local band-to-band tunneling model [18,19] that accounts for arbitrary tunneling barrier with non-uniform electric field is employed. Local tunneling models such as Hurkx [20] and Schenk [21] models assume a constant electric field along the tunneling path. In the non-local band-to-band tunneling model, the electric field at each point along the tunneling path is dynamically changing. The tunneling current is calculated with each point of the band profile. In this framework, the tunneling paths are dynamically calculated according to the gradient of energy band. Similar to the work in [11], the parameters in the non-local band-to-band tunneling model are calibrated with the data in [22]. In addition, to accurately describe the analog behavior of FinFET devices, the mobility model has also been calibrated [23]. Fig. 1 shows a schematic of the simulated double-gate structure for TFET and FinFET devices, which are designed with similar device geometries (L_g = 25 nm, W_{fin} = 7 nm, H_{fin} = 20 nm, and EOT = 0.65 nm). As can be seen in Fig. 2, the TFET device with steeper subthreshold slope possesses lower V_T (~0.27 V) than that of FinFET (~0.33 V) while maintaining comparable I_{OFF}. Besides, we utilize asymmetric source/drain doping ($N_{source} = 3 \times 10^{20}$ cm^{-3} and $N_{drain} = 1 \times 10^{20}$ cm^{-3} [6]) for TFET to mitigate the drain-side ambipolar leakage. A graded junction

* Corresponding author.
E-mail address: pinsu@faculty.nctu.edu.tw (P. Su).

http://dx.doi.org/10.1016/j.microrel.2014.11.012
0026-2714/

(1 nm/decade doping decay) for the source–channel and drain-channel junctions is applied in this work.

Since analog circuits are usually biased in the low gate-bias regime for better power efficiency [24,25], we focus on the analog FOMs at gate-voltage overdrive V_{GT} = 0.2 V ($V_{GT} = V_{GS} - V_T$). Fig. 3 shows a comparison of the output resistance (R_{out}) versus V_{DS} characteristics for the TFET and FinFET devices biased at V_{GT} = 0.2 V. It can be seen that the R_{out} of TFET reaches its maximum for V_{DS} larger than ~0.6 V. Therefore, in this work, we examine the impact of random variability on important analog FOMs for devices biased at V_{GT} = 0.2 V and V_{DS} = 0.6 V.

For the variability analysis, the WFV resulting from the poly-grain characteristic of metal gate is considered as the main variation source. To simulate the random grains of the metal gate, the Voronoi approach [13] that can faithfully imitate the irregular grain patterns is employed for TiN metal gate with 5 nm average grain size [14]. To simulate WFV by Voronoi approach [13], we distribute grain seeds randomly first. The number of grain seeds is equal to the metal area divided by the average size. Then, we draw the perpendicular bisector between each two seeds. The area ringed by the perpendicular bisector is the grain. Fig. 4(a) shows the formation of Voronoi pattern for WFV. Finally, we assign WF on these grains based on the probability of each orientation as shown in Fig. 4(b).

For the TiN metal gate, two grain orientations (⟨200⟩ and ⟨111⟩) with 60% and 40% occurring probabilities, respectively, are considered [16], and the work function of ⟨200⟩ is 0.2 eV higher than that of ⟨111⟩ [11,13,16]. To capture the statistical characteristics of TFET and FinFET devices due to WFV, 3-D TCAD atomistic simulations are performed. Fig. 1 shows a simulated device structure with Voronoi grain pattern representing the WFV.

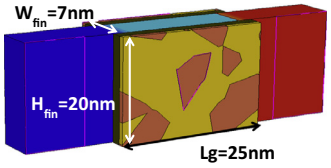
3. Results and discussion

Fig. 5 shows the WFV-induced dispersions of I_{DS}–V_{GS} for TFET and FinFET devices at V_{DS} = 0.6 V. Compared with FinFET, it can be seen that TFET exhibits larger I_{DS} fluctuation at lower V_{GS}. In addition, it is noted that TFET exhibits larger subthreshold-swing variation as compared with the FinFET counterpart.

In Fig. 6, the normalized g_m variations of TFET and FinFET are compared. It can be observed that TFET and FinFET devices exhibit comparable variability σ/μ, which is the normalized standard deviation and an indicator of FOM variation [26].

$$\frac{\sigma}{\mu} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \mu)^2}}{\mu} \quad (1)$$

where σ represents the standard deviation of FOM distribution and μ represents the mean value of FOM distribution. N is the sample number, which is equal to 150 in this study.



Doping Concentration		
	TFET (p-i-n)	FinFET (n-i-n)
Source	3e20 cm^{-3}	1e20 cm^{-3}
Drain	1e20 cm^{-3}	1e20 cm^{-3}
Doping decay	1 nm/decay	
WFV Simulation		
Modeling approach	Voronoi	
Average grain size	5 nm	
Tunneling orientation	<110>	

Fig. 1. Schematic of the simulated double-gate structure for TFET and FinFET taking metal-gate WFV with Voronoi grain pattern into consider [13]. L_g is the gate length, W_{fin} is the fin width, and H_{fin} is the fin height. This table shows conditions for doping and WFV simulation.

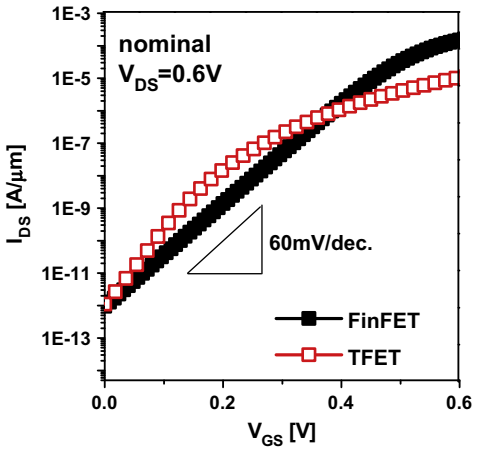


Fig. 2. I_{DS}–V_{GS} characteristics of the TFET and FinFET devices at V_{DS} = 0.6 V. The threshold voltages (V_T) are 0.27 V and 0.33 V, respectively, for TFET and FinFET with a constant current equal to 10^{-7} A/μm.

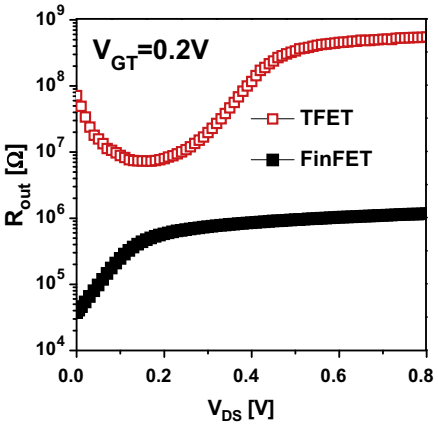


Fig. 3. Comparison of the output resistance versus V_{DS} characteristics for the TFET and FinFET devices biased at V_{GT} = 0.2 V.

In g_m, while FinFET possesses about one-order-of-magnitude larger g_m than that of TFET [7]. However, as indicated in Fig. 7, the advantage of FinFET against TFET in g_m/I_{DS} is marginal. Fig. 7 also shows that TFET possesses smaller variability in g_m/I_{DS} as compared with the FinFET counterpart.

Fig. 8 shows the normalized R_{out} distributions for TFET and FinFET at V_{GT} = 0.2 V and V_{DS} = 0.6 V. It can be seen that, in addition to offering a substantially higher output resistance (about two-orders-of-magnitude higher in μ) [7], TFET also possesses smaller R_{out} variation (σ/μ) as compared with FinFET. This can be explained as follows. For FinFET, the output resistance is quite sensitive to the gate work-function near the drain side because it may determine the inversion charge near the drain and thus the screening of drain-field penetration (i.e., the degree of DIBL) [27]. For TFET, however, the band-to-band tunneling current generated through the source–channel junction is less sensitive to the drain field and thus the drain-side work function.

Fig. 9(a) shows the normalized intrinsic-gain ($g_m \times R_{out}$) variations for TFET and FinFET. It can be seen that, in addition to providing a larger intrinsic gain (~3× in μ), TFET also exhibits smaller intrinsic-gain variation (σ/μ) as compared with FinFET. Although the g_m variation is comparable, a smaller R_{out} variation (Fig. 8) results in the smaller intrinsic-gain variation for TFET. Furthermore, the strong negative correlation between g_m and R_{out}