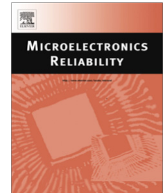
Microelectronics Reliability 55 (2015) 337–341

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



# Investigation on the origin of the anomalous tail bits on nitrided charge trap flash memory

Meng Chuan Lee *, Hin Yong Wong

*Faculty of Engineering, Multimedia University, Persiaran Multimedia, 63100 Cyberjaya, Selangor, Malaysia*

ARTICLE INFO

*Article history:*
Received 13 August 2014
Received in revised form 7 October 2014
Accepted 22 October 2014
Available online 15 November 2014

*Keywords:*
Anomalous tail bits
Nitrided flash memory
Reliability analysis
Threshold voltage instability
Trap-assisted-tunneling

ABSTRACT

In this work, the origin of the anomalous tail bits have been examined thoroughly on 43 nm nitride based charge trap flash memory devices. Tunnel oxide nitridation was implemented on the device under study to enhance its immunity to charge loss mechanism. Due to the extensive program/erase cycling, the increment in the defect density in tunnel oxide layer has generated significant tail bits that exhibited detrimental charge loss at room temperature. The findings have indicated that these tail bits are attributed to randomly distributed defects due to extensive program/erase cycling stress. Furthermore, these tail bits enhanced with longer storage duration at room temperature but deterred at high storage temperature. In this work, the anomalous tail bits were suppressed at high storage temperature. The underlying physical mechanism for these anomalous tail bits was found to be attributed to trap-assisted-tunneling mechanism that enables trapped charges from nitride storage layer to leak out along the vertical path of oxide–nitride–oxide stack of nitrided flash memory. These findings have implied that the anomalous tail bits are one of the critical reliability concerns that need to be addressed to achieve desired reliability performance. This work also demonstrated that room temperature storage test is a critical test to investigate the generation of the detrimental anomalous tail bits in reliability characterization and qualification for future nitrided flash memory.

© 2014 Elsevier Ltd. All rights reserved.

## 1. Introduction

Since the invention of flash memory by Dr. Fujio Masuoka in 1981, flash memory is one of the key enablers to realize the modern day's information technology (IT) products, such as smart phones and mobile computing devices. Typical flash memory devices are Floating Gate (FG) flash memory and nitride based charge trap flash (NBCTF) memory. The injected charges are stored in conductive poly silicon FG and discrete inherent trap sites of nitride layer respectively. In order to consistently push for lower average cost per bit of high density flash memory, technology scaling is implemented aggressively on flash memory devices that will miniaturize the flash memory cell's dimensions while maintaining good data retention capability. This technology scaling method enables more memory transistors to be fitted into smaller design floor space. This will increase the storage space of flash memory to meet the growing need for larger memory space in the market. Nevertheless, there are three critical limitations that prevent further technology scaling on FG flash memory, i.e. (1) severe stress induced leakage current (SILC) triggered if the tunnel oxide layer is scaled to less than 8 nm; (2) gate coupling ratio of minimum 0.6 has to be met in order for control gate of FG flash memory to properly exert control to FG and the channel; (3) severe cell-to-cell interference [1–8]. As compared to FG flash memory, NBCTF memory enables better downscaling of the tunnel oxide layer while still preserving overall good data retention performance. However, the downscaling of tunnel oxide layer of NBCTF memory has to be complemented with innovative approaches to continue the technology scaling trend for NBCTF memory [3,4]. Tunnel oxide nitridation (TON) is one of the approaches applied together with the downscaling of tunnel oxide layer in order to enhance the immunity of NBCTF memory to Fowler–Nordheim (FN) stress induced damages in tunnel oxide layer. By implementing various wet or dry nitridation processes, TON is done by incorporating nitrogen content into the tunnel oxide layer to achieve larger memory window and better hardening towards the damages due to extensive program/erase P/E) cycling stress through FN injection [1–10]. Nevertheless, TON was also found to result in several critical reliability issues such as Fermi-level defects and mid-gap defects. These defects would then lead to random telegraph noise and quick electron de-trapping respectively [4,9–11]. In our previous work, TON was found to modulate dominant charge loss (CL) mechanism from high temperature charge loss (HTCL) that

* Corresponding author.
*E-mail address:* mclee1321@gmail.com (M.C. Lee).

http://dx.doi.org/10.1016/j.microrel.2014.10.013
0026-2714/© 2014 Elsevier Ltd. All rights reserved.

resulted in uniform threshold voltage (Vt) distribution shift to room temperature charge loss (RTCL) as a result of the generation of severe anomalous tail bits [9]. In this work, the origin of the anomalous tail bits is examined and studied. Moreover, the dependency of the anomalous tail bits to storage temperatures is investigated on nitrided NBCTF memory. Furthermore, the effect of P/E stress to the anomalous tail bits is also thoroughly investigated by performing systematic experiments on nitrided NBCTF memory. Based on the experimental findings, the origin and the underlying physical mechanism of these anomalous tail bits on nitrided NBCTF memory are deliberated in this work.

## 2. Experimental

As shown in Fig. 1, the devices under study were 43 nm NBCTF memory devices that consists of poly silicon gate, top silicon oxide layer, silicon nitride layer, tunnel silicon oxide layer and silicon substrate. The layers between the poly silicon gate and substrate form the oxide–nitride–oxide (ONO) stack of the NBCTF memory cell. The physical thicknesses for each layer of the ONO stack were 8, 7, 5.5 nm. The silicon nitride layer acts as the designated charge trap layer which is sandwiched between the top silicon oxide layer and tunnel silicon oxide layer. The intrinsic defects in silicon nitride layer which surrounded by oxide layers inherently trap injected charges during P/E operations [1–4]. The top and tunnel silicon oxide layers provide sufficient protection to prevent charge leakage due to direct tunneling of charges from silicon nitride layer. Nitridation was performed on tunnel oxide layer by annealing the grown tunnel oxide layer in nitric oxide ambient thereby incorporating the nitrogen content into the tunnel oxide layer. The memory density of the device used in this study is 0.5 million bits per block and total 100 blocks were used. Program and erase operations of this device were performed by implementing FN tunneling mechanism to inject electrons and holes into the silicon nitride layer until the memory cell's Vt reached the target Vt level. Vt measurements were taken on all memory devices used in this study before P/E cycling.

A set of functional memory devices were cycled repeatedly by programming zeros pattern and erasing them to uniformly induce damages onto the tested memory devices. In this work, a total of 8000 P/E cycle counts were implemented on a set of nitrided NBCTF memory devices to investigate the effect of P/E cycle count to the CL mechanism. The P/E cycling was performed at room temperature, i.e. 25 °C in order to avoid the recovery of P/E cycling induced damages if P/E cycling was performed at higher cycling temperature. Another set of functional memory devices were not cycled. After the completion of P/E cycling, Vt data was collected on all memory cells from both sets of memory devices. Subsequently, both sets of the memory devices were stored at 25, 55, 90, 125, and 175 °C. At each read point, i.e. time 0, 0.1, 1, 24, 100 and 500 h, Vt per bit measurements were collected on both sets of the memory devices. To further investigate the origin of tail bits, all devices were erased and programmed for one time. Vt per bit was then measured for 100 P/E cycled blocks on all devices. Once it is completed, both set of devices were annealed for 24 h before Vt per bit data was measured again. The sequence of erase/program and Vt measurement before and after 24 h at room temperature was repeated for 6 times to count the number of tail bits repeated in each sequence.

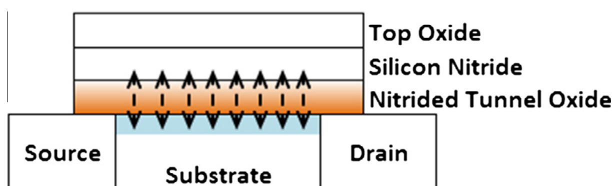



**Fig. 1.** Typical cell structure of nanoscale nitrided NBCTF memory with single bit per cell architecture.

## 3. Results and discussions

To track the growth of the anomalous tail bits, Vt per bit measurements collected at all read points were used to calculate the Vt shift by subtracting the Vt per bit at each read point with the Vt of the same bit (the bit is identified by its physical location) at time 0 h which is before bake. In this work, the bits that have Vt shift of more than or equal to 0.2 A.U. are categorized as anomalous tail bits. This is because the resolution of Vt measurement used in this study is 0.025 A.U. per step. The Vt measurement range used in this work is 0 A.U. to 4.5 A.U. Vt fluctuation is 8 times of the resolution. Therefore, a bit that exhibits 0.2 A.U. fluctuations is considered as a tail bit with anomalously large Vt fluctuation as compared to the rest of the bits. Based on Vt per bit measurements collected at every read point throughout this work, anomalous tail bits were observed to perturbed from Vt distribution at room temperature as compared to high storage temperature. Fig. 2 shows the generation of anomalous tail bits is enhanced for lower storage temperature and peaked at room temperature, i.e. 25 °C. This clearly depicts that the generation of the anomalous tail bits favoured room temperature and enhanced with longer storage durations.

Fig. 3(a) and (b) show the Vt distribution plotted for P/E cycled blocks stored at 25 °C and 175 °C. As shown in Fig. 3(a), significant number of tail bits was observed to be generated and enhanced at the low end of the distribution of programmed bits when the devices are stored at 25 °C. By comparing the Vt distributions shown in Fig. 3(a) and (b), the entire Vt distribution of programmed bits does not shift significantly as storage duration increases at 25 °C. Furthermore, the number of tail bits was observed to gradually increase as storage duration prolongs at 25 °C. This observation indicates that the underlying CL mechanism impacts only on a small portion of the programmed bits at 25 °C. On the contrary, the entire Vt distribution of programmed bits was observed to be shifted significantly to lower Vt level when the storage duration at 175 °C prolongs as shown in Fig. 3(b). Furthermore, as shown in Fig. 3(b), the generation of tail bits is not observed at 175 °C but uniform Vt distribution shift is observed on nitrided NBCTF memory. This observation indicates that the CL mechanism at 175 °C impacts all programmed bits. By comparing Fig. 3(a) and (b), the observations on the CL behaviour exhibited by the distinct Vt distribution shift implies the underlying physical mechanism attributed to the CL mechanism observed at 25 °C is different than at 175 °C.

Fig. 4 shows the trend of average tail bits as a function of storage durations at room temperature and high storage temperature, i.e. 175 °C. The average tail bits per block was calculated by

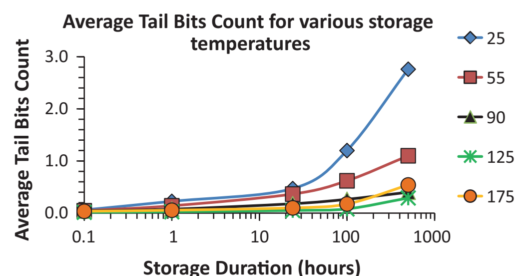



**Fig. 2.** Average tail bits count per 100 P/E cycled blocks is plotted as a function of various storage temperatures.

Download English Version:

https://daneshyari.com/en/article/548143

Download Persian Version:

https://daneshyari.com/article/548143

Daneshyari.com