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All-digital thermal distribution measurement on field programmable gate array using ring oscillators

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ABSTRACT

In this paper, a digital method for transient temperature distribution measurement of field programmable gate array (FPGA)-based systems is proposed. The smart thermal sensors used rely on correspondence between the delay and temperature in a ring oscillator. The tested temperature was converted into a time signal with a thermally-sensitive width. The output frequency is read out by a counter with a scan path, and then, transited to PC by a Universal Serial Bus (USB) interface. We capture the infrared images of the FPGA chip by infrared camera. The images were compared with the thermal map of the die constructed using an array of sensors. The tested temperature error varies by less than 1.6 °C in the range from 20 °C to 90 °C, and the maximum sampling rate is 330 Hz.

1. Introduction

Field programmable gate array (FPGA)-based system device structures are shrinking while their device densities are increasing, meaning that thermal management is gaining increasing importance in these structures [1]. High temperature affects the performance of circuits, which can lead to timing errors and reduced reliability [2]. While methods are available to gather the thermal information, like embedded diodes available in FPGAs or use of infrared imagers [3,4], these methods are not suitable for use in that embedded diodes can get the temperature at points in the die, and infrared imagers are rarely used for their expensive and destructive causes. Therefore, the smart thermal sensor has been proposed, which can enable measurement of the junction temperature distribution rather than single position temperature of the package.

Numerous ring oscillator-based thermal sensors have been described in the literature previously [5–8], but the detailed studies have been rarely performed to date. Datta and Burleson [13] proposed use of differential ring oscillators (DRO) for thermal sensing, but its sensing design depended on full-custom which made it hard to adapt to process variation. The differential ring oscillators are fixed in a certain position of the die. In [5] the authors proposed temperature sensors based on ROs. The system calibrated them using an internal precalibrated thermal diode on a Virtex-6 FPGA.

In this paper, an array of sensors is used to construct a thermal map of the die to measure its temperature distribution and to predict the transient thermal behavior of the FPGA-based system. The sensors are fully digital and constructed by pure standard cell-based design that can be dynamically inserted and eliminated at any position of the die. The proposed all-digital thermal sensor can be used to get transient thermal distribution of the die. We also captured the infrared images of the package for comparison with the measured results of the sensors in order to calibrate the thermal sensor and to improve the accuracy by evaluating the influence of the number of inverters.

2. Smart thermal sensor

The smart thermal sensor consists of a thermally sensitive ring oscillator, which is a circular chain with an odd number of inverters, as shown in Fig. 1. The oscillation period is twice the sum of the delays, and is given as [9]:

$$f_{out} = \frac{1}{2N \cdot T_d} \tag{1}$$

where N is the number of inverters resident in the ring oscillator, and T_d is the average propagation delay. By neglecting the effects of velocity saturation, channel length modulation and other non-idealities for simplicity, the propagation delay under the first-order approximation can then be given as [10]:

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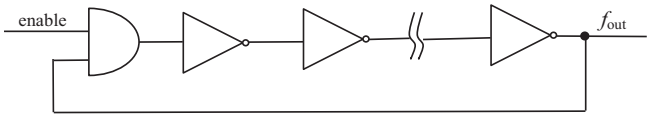

Fig. 1. Schematic of the ring oscillator.

$$T_d = \frac{(L/W)C_L}{\mu C_{ox}(V_{DD} - V_T)} \ln\left(\frac{1.5V_{DD} - 2V_T}{0.5V_{DD}}\right) \quad (2)$$

The length/width ratio L/W, the gate oxide capacitance C_{ox} and the effective load capacitance C_L are independent of the temperature, while the thermal characteristics of the mobility μ and the threshold voltage V_T change with temperature, and can be derived as follows [11]:

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{km} \quad (3)$$

$$V_T(T) = V_T(T_0) + \alpha(T - T_0) \quad (4)$$

In the majority of designs, the supply voltage is chosen to be high enough that $V_{DD} \gg V_T$. Under these conditions, the delay becomes virtually independent of the supply voltage, and the electron mobility plays the main role in thermal effects of the propagation delay. The threshold voltages of transistors for Altera FPGA are 100 mV, the supply voltage is 3.3 V which is much greater than the threshold voltage. Because of the negative temperature coefficient of the surface carrier mobility for electrons, the propagation delay T_d has a positive temperature coefficient. This means that as the temperature increases, then the output frequency of the ring oscillator decreases.

The block diagram of the smart thermal sensor is depicted in Fig. 2. The thermal sensor converts temperature into time information being fed into a time-to-digital converter according to a reference clock for digital coding. The ring oscillator translates the tested temperature into a pulse with a temperature-proportional width. A counter with a scan path captures the frequency over a fixed pulse to produce the digital output which is transmitted to the computer through the Universal Serial Bus (USB) interface. The fixed period is provided by the system clock, and it is useful to increase the wiring delays and thus reduce the operating frequency of the ring oscillator; in this case, the goal is to make the operating frequency lower than that of the system clock to minimize self-heating [11].

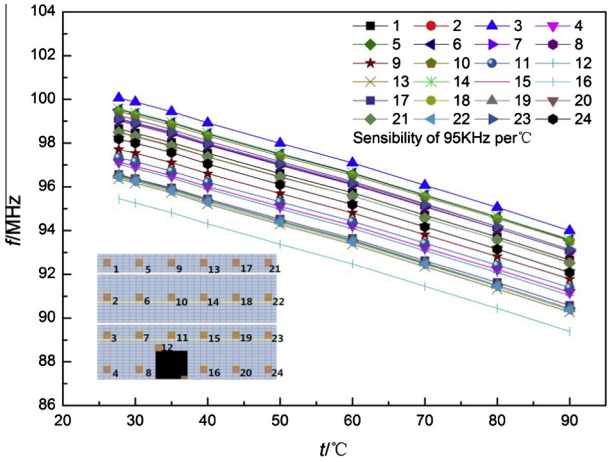

Fig. 3. Sensor output frequency dependence on temperature.

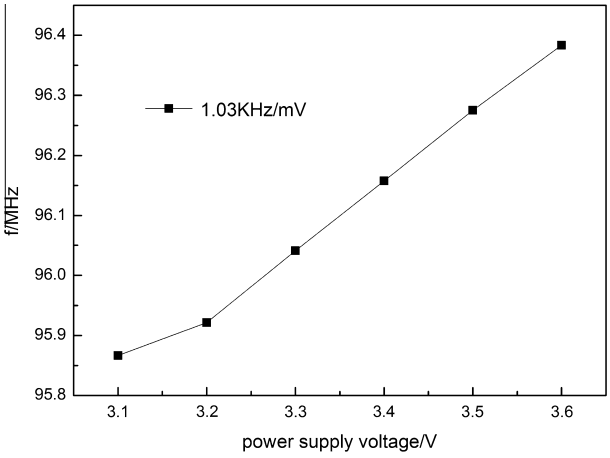

Fig. 4. Sensor output frequency dependence on power supply voltage.

3. FPGA implementation

An Altera Cyclone III series FPGA chip is used for circuit realization to verify the proposed thermal sensor. A ring oscillator is constructed using inverters, which can be mapped on the FPGA using the look-up tables (LUT); the logic utilization for such a sensor is as low as 21 logic elements (LE). A delay line can be built among the

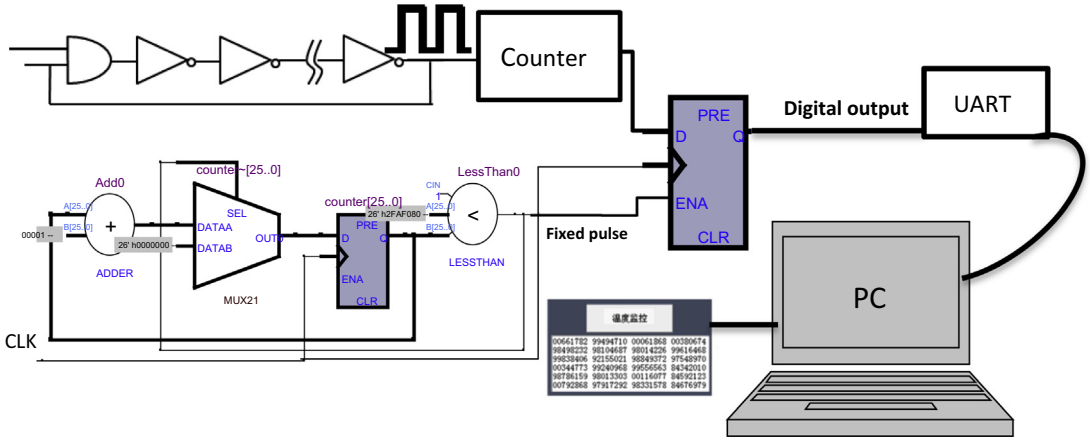

Fig. 2. Block diagram of the thermal sensor.