Microelectronics Reliability 54 (2014) 629–632

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Effect of polyimide baking on bump resistance in flip-chip solder joints

Hsi-Kuei Cheng [a], Shien-Ping Feng [b], Yi-Jen Lai [c], Kuo-Chio Liu [c], Ying-Lang Wang [d,*], Tzeng-Feng Liu [a,*], Chih-Ming Chen [e,*]

[a] Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[b] Department of Mechanical Engineering, The University of Hong Kong, Pokfulam, Hong Kong
[c] Backend Operations Division, Taiwan Semiconductor Manufacturing Company (TSMC), Ltd., Taiwan
[d] Institute of Lighting and Energy Photonics, National Chiao Tung University, Hsinchu 300, Taiwan
[e] Department of Chemical Engineering, National Chung Hsing University, Taichung 402, Taiwan

ARTICLE INFO

Article history:
Received 12 December 2012
Received in revised form 12 November 2013
Accepted 12 November 2013
Available online 2 December 2013

ABSTRACT

The effect of polyimide (PI) thermal process on the bump resistance of flip-chip solder joint is investigated for 28 nm technology device with aggressive extreme low-k (ELK) dielectric film scheme and lead-free solder. Kelvin structure is designed in the bump array to measure the resistance of single solder bump. An additional low-temperature pre-baking before standard PI curing increases the bump resistance from 9.3 mΩ to 225 mΩ. The bump resistance increment is well explained by a PI outgassing model established based on the results of Gas Chromatography–Mass Spectrophotometer (GC–MS) analysis. The PI outgassing substances re-deposit on the Al bump pad, increasing the resistance of interface between under-bump metallurgy (UBM) and underneath Al pad. The resistance of interface is twenty-times higher than pure solder bump, which dominates the measured value of bump resistance. Low-temperature plasma etching prior to UBM deposition is proposed to retard the PI outgassing, and it effectively reduces the bump resistance from 225 mΩ to 10.8 mΩ.

1. Introduction

Flip-chip package is the most important assembly method over the last decade especially for advanced fine-pitch devices [1,2]. Large number of tiny solder bumps are fabricated into an area array on a chip, where the bump plays an important role to connect the input/output (I/O) electronic signal between the chip and a package substrate. The diameter of the solder bumps is 100 m or less, and it continues to shrink for the purpose of small size and light weight. Typically, the resistance of a solder bump is estimated to be the order of few milli-ohms, whereas the resistance of the metallization trace ranges from few hundreds to few thousands of milli-ohms, depending on its dimension [3]. In general, the bump resistance is quite small compared with the resistance of the metallization traces. However, if the bump resistance is rose to few hundreds of milli-ohms, it will affect the transmission speed due to RC time delay.

Bump resistance measurement is a non-destructive detection which is usually used to monitor the tiny defect formation or microstructure changes in the solder bumps, especially for the investigations of bump reliability issues such as electromigration (EM) and temperature cycle (TC). Many literatures discussed the bump fatigue behavior during the reliability tests. The formation of voids and cracks in the solder bump induced bump resistance changes [4–7]. The Kelvin structure is designed in the ball grid array to measure the bump resistance and monitor the failure of EM and TC tests in flip-chip package. The bump resistance is increased gradually with increasing the stress time and finally opens while the solder bumps fail.

In this paper, we investigated the bump resistance changes with a polyimide (PI) layer covered on the chip surface. The purpose of PI layer is to release the thermal stress of solder bump and underneath extreme low-k (ELK) dielectric film during TC test. Typically, the PI film undergoes a curing process after photo development. An additional low-temperature pre-baking prior to curing was employed because it effectively enlarged the window of chip–package interaction (CPI) of flip-chip package especially for lead-free (LF) SnAg bumps. However, the pre-baking step caused a significant increment of the bump resistance. A mechanism of PI outgassing was proposed to explain the bump resistance increment based on the results of Gas Chromatography–Mass Spectrophotometer (GC–MS) analysis and an experiment of PI removal thickness on the bump resistance. This study provided a deeper understanding of the bump resistance change for LF flip-chip bump, and the results implied the bump resistance was a good indicator to monitor tiny abnormality of Fab PI process and bumping under-bump metallurgy (UBM) sputter process.

* Corresponding authors. Tel.: +886 6 3032535 (Y.L. Wang), tel: +886 3 5712121 31288 (T.F. Liu), tel.: +886 4 22859458 (C.M. Chen).
E-mail addresses: ylwang@tsmc.com (Y.-L. Wang), tfliu@cc.nctu.edu.tw (T.-F. Liu), chencm@nchu.edu.tw (C.-M. Chen).

0026-2714/$ - see front matter © 2013 Published by Elsevier Ltd.
http://dx.doi.org/10.1016/j.microrel.2013.11.006

2. Experimental procedures

The test vehicle employed in the bump resistance experiment was a 10 mm × 9 mm die that covered a HD4104 PI film on the top of chip. Photo development was performed on the PI film to form a circular opening on designed Al pad for subsequent UBM deposition. Prior to UBM deposition, two thermal processes of PI film were applied: mode-I was direct curing at 380 °C for about 2 min; mode-II was pre-baking the PI film at 200 °C for about 15 min before curing at 380 °C. After the PI thermal process, argon plasma etching at 250 °C for about 1 min was employed for surface cleaning. GC–MS was used to analyze the outgassing characteristics of the PI films thermally treated by two different modes mentioned above. It is a method that combines the features of gas–liquid chromatography and mass spectrometry to identify different substances within a test sample. Subsequently, Ti and Cu films were sequentially deposited on the Al pad using sputtering as the barrier and seed layers, respectively. Electroplating Ni UBM and LF SnAg (Ag = 1.8%) solder bump were made as the connection between the chip and a package substrate.

The Kelvin structure was designed in the bump array to monitor the resistance of single solder bump. A schematic drawing of the solder bump and Kelvin structure is shown in Fig. 1. The three solder bumps were connected by one Al metal line. A current (I_{12}) was forced through contact pin 1 to pin 2, and the voltage difference (ΔV_{34}) between contact pins 3 and 4 was detected. The resistance of single bump can be calculated as $\Delta V_{34}/I_{12}$.

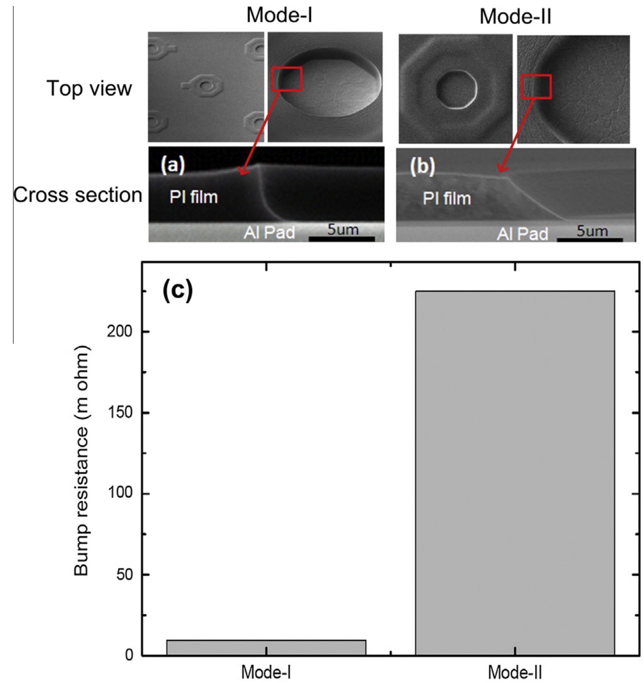

Fig. 2. Cross-sectional SEM images of PI opening for (a) mode-I and (b) mode-II. (c) Bump resistance measurement values of two different modes of PI thermal process.

3. Results and discussion

Fig. 2(a) and (b) shows the cross-sectional scanning electron microscopy (SEM) images of PI opening in mode-I and mode-II samples, respectively. It was found that the PI film shrunk slightly on the top of the opening as seen in Fig. 2(b) for mode-II sample, resulting in an increase of diameter at the top opening. Based on top-view observation, the diameter of the PI opening were comparable at the bottoms for both mode-I and mode-II samples (~30 m), but the top of the opening of mode-II sample was larger than mode-I by about 4 m in the diameter because the additional pre-baking resulted in slight PI film shrinkage. Considering the reliability issue of LF SnAg solder bump in advanced flip-chip package, the PI profile at the opening side is preferred to rounding shape as mode-II shown in Fig. 2(b). This is because a rounding shape of the PI opening side caused by an additional pre-baking at 200 °C can enlarge CPI window. The additional pre-baking employed in mode-II thermal process can also remove the moisture in the PI film. However, a side effect was found according to the results of bump resistance analysis. As the same scheme for flip-chip bump, the bump resistance of mode-II sample was rose twenty-time higher than that of mode-I one as shown in Fig. 2(c). The twenty-time increment in bump resistance should not be caused by the profile change of PI opening because the contribution of profile change is only the order of few milli-ohms. On the other hand, if the profile change of PI opening indeed affects bump resistance, the bump resistance should reduce for mode-II sample because of a larger area of the opening. Therefore, it implied that some other issue instead of the opening profile change was responsible for the resistance change and this issue should closely relate to the additional PI pre-baking at 200 °C employed in mode-II thermal process.

In addition to profile change of PI opening, pre-baking of the PI film at 200 °C for a relatively longer time (15 min) might also cause prominent degassing of some photosensitive and polymer compounds out of the PI film. To analyze the degassing phenomenon, the sample pre-baked at 200 °C was examined using GC–MS and the result was shown in Fig. 3(a). It was found that H_2O, CO, CO_2, photo-sensitive and monomer were diffused out of the PI film after pre-baking at 200 °C (mode-II). The PI film after 380 °C curing (mode-I) was also examined using GC–MS and only few H_2O, CO and CO_2 were released because of a shorter curing time (2 min) as seen in Fig. 3(b). Based on the above results of GC–MS analysis, a model of PI outgassing was proposed to explain the mechanism of the resistance difference between mode-I and mode-II PI films. Fig. 4(a)–(c) represent the PI status at each step in mode-I thermal process. After photo development, unstable substances, say, outgassing source like solvent and partial-linked PI, were uniformly distributed in the PI film as the solid spots in Fig. 4(a). The uniform distribution of unstable substances could be approximately

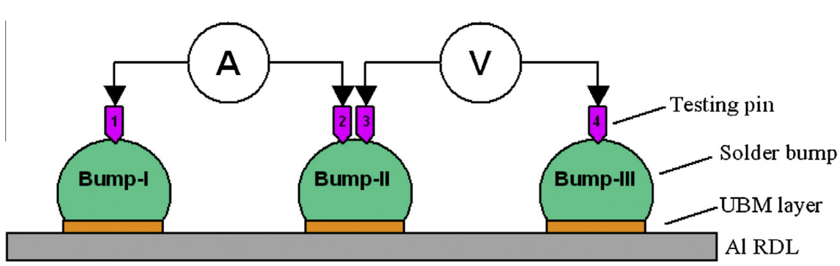

Fig. 1. Schematic diagram of solder bump and Kelvin structure.