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A finite state machine based fault tolerance technique for sequential circuits

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ABSTRACT

With technology advancement at the nanometer scale, systems became more subjected to higher manufacturing defects and higher susceptibility to soft errors. Currently, soft errors induced by ion particles are no longer limited to a specific field such as aerospace applications. This raises the challenge to come up with techniques to tackle soft errors in both combinational and sequential circuits. In this work, we propose a finite state machine (FSM) based fault tolerance technique for sequential circuits. The proposed technique is based on adding redundant equivalent states to protect few states with high probability of occurrence. The added states guarantee that all single faults occurring in the state variables of highly occurring states or in their combinational logic are tolerated. The proposed technique has minimal area overhead as only few states need protection.

1. Introduction

Probability of failure of digital systems grows in direct proportion to Moore's law [1]. Continuous improvements in CMOS technology entering the nanometer scale has resulted into quantum mechanical effects creating many technological challenges for further scaling of CMOS devices. This has led to the exploration of new technologies for circuit design. Nanotechnology-based fabrication is expected to offer the extra density and potential performance to take electronic circuits the next step. It is estimated that molecular electronics can achieve very high densities (10^{12} devices per cm^2) and operate at very high frequencies (of the order of THz) [2]. Nano-scale devices are limited by higher defect rates and increased susceptibility to soft errors. The reduced noise tolerance of these devices is responsible for inducing device malfunctions by external influences like EMI, thermal perturbations and cosmic radiations.

Temporal transient faults (soft errors) can hit either in the combinational logic or flip flops of a sequential circuit. If the error occurs in the combinational logic, it will result in *Single Event Transient* (SET). On the other hand, if it occurs in the memory cell itself, it will result in a *Single Event Upset* (SEU). Both of SET and SEU cause a major implication in sequential circuit and should receive a proper treatment. Transient faults (SET/SEU) are mainly caused by ions movement through the materials of ICs. With feature sizes reaching below 0.35 μm, SET and SEU faults are no longer considered a small attenuation. Instead they will be considered as normal circuit signals. Soft Error Rate (SER) will grow in direct proportion to the number of cells in the design and with reduction in voltage [3].

Fortunately, there are some masking properties that prevent transient faults from affecting sequential circuits, namely: *logical masking*, *electrical masking* and *latching window masking*. Logical masking prevents the SET from propagating from the fault location to a circuit output due to the logic of the circuit. For example, a 2-input AND gate can mask any fault in one input if the other input has a "0" value. Electrical masking attenuates or completely masks the SET signal due to electrical properties of gates. Latching window masking occurs due to the arrival of the transient pulse outside the latching window for the memory element. However, the reduction in feature sizes limits the effect of electrical and latching window masking.

In order to overcome the soft errors effect problem in sequential circuits, several techniques have been proposed in the literature. Triple Modular Redundancy (TMR) is one of the well known techniques to reduce the impact of soft errors in combinational logic. In TMR, all the three identical modules perform the same operation, and a voter accepts outputs from all three modules, producing a majority vote at its output. If a single voter is used, that voter becomes a critical point of failure and the reliability of the TMR structure is limited by that of the final arbitration unit (i.e., voter). Despite this limitation, TMR is heavily used in practice whenever the reliability of the circuit is a crucial demand especially when single faults are needed to be protected. In [4], a TMR hardening technique addressing SEU faults is proposed based on a temporally redundant sampling latch.

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In [5], it is concluded that 49% of the overall soft errors for a design manufactured using state of the art technologies result from sequential elements. Hence many proposed techniques are based on latch hardening techniques which provide tolerance for faults occurring in memory elements. Examples of these techniques are given in [6–9].

The work in [10] proposes the use of duplication with self-checking for one-hot encoding FSM. This approach ensures that any single error will not lead to an incorrect next state. However, it might lead to an erroneous output. The area overhead of this approach is considered large as two sets of selectors are used and each selector set is equal to the number of flip–flops, which is equal to the number of states. The work in [11] addresses the fault tolerance of FSMs based on N-modular redundancy by adding N voters instead of one voter to tolerate errors occurring in the voters. It also guarantees that any single error will not lead to an incorrect next state. However, it might lead to an erroneous output. In [12], it is shown that for a given ability to tolerate faults, fault tolerance based on replication yields better circuit reliability than based on error correcting codes. However, for a given area complexity, error correcting codes based on orthogonizable codes provide better reliability than replication. In [13], a novel reduced m out of n coding method is proposed that can be used for the synthesis of a totally self checker for tolerating soft errors. The authors propose totally self-checking synchronous sequential circuits that are able to recover after an occurrence of a fault.

Rollback recovery is one of the techniques that can be used for fault tolerance. It brings the circuit back several cycles to a state it has reached in the past and requires to store the state of the circuit at some cycle boundaries. In [14], a model that deals with Multiple Bit Upsets (MBUs) is proposed to study the impact of MBUs on the reliability of rollback recovery circuits.

The objective of this work is to investigate the design of fault tolerant sequential circuits based on adding redundant states at the state diagram level. The objective of adding redundant states is to guarantee tolerance of all single soft errors of states with high probability of occurrence. Since steady state probability for several sequential benchmark circuits have significant variance, our method takes advantage of that and chooses some of the states with high probability of occurrence for protection. This way the area overhead is kept minimal.

The rest of the paper is organized as follows. Section 2 describes the proposed FSM-based fault tolerance technique. Section 3 describes the simulation framework used to evaluate circuit failure probability and reliability. Section 4 presents the results of the proposed technique as well as a comparison with existing fault tolerance techniques in terms of both failure rate and area. The paper finally concludes with Section 5.

2. Proposed finite state machine based fault tolerance technique

In this section, we will introduce a novel idea to increase sequential circuit reliability based on adding redundant equivalent states to the states with high probability of occurrence. By protecting states with high probability of occurrence, the reliability of a sequential circuit is increased as it is very likely that the error occurs when the circuit is either in one of these states or going to one of them. The newly added redundant states are equivalent to the protected states and are assigned the same next state and output.

2.1. Type of states in fault tolerant sequential circuit

States in a fault tolerant sequential circuit can be classified into three types: normal states, protected states, and redundant states. Normal states are original states that are not protected for fault tolerance. Protected states are states that will be considered for reliability enhancement due to their high probability of occurrence. For each protected state, equivalent redundant states will be added to guarantee single soft fault tolerance. Fig. 1 illustrates an example that shows different types of states. There are 3 original states in Figs. 1 and 2 of them are protected and 1 is normal. Each of the 2 protected states has 4 redundant equivalent states. The number of redundant states added will be the minimum number required to satisfy fault tolerance as will be discussed in Section 2.3.

2.2. State probability calculation

In order to decide which of the original states of a finite state machine need to be protected, states must be sorted based on their probability of occurrence. Probabilistic approaches try to correlate the various probabilities in order to calculate steady state probabilities if the FSM is simulated for infinite amount of time.

Logic synthesis [15], verification [16], testing [17,18] and low-power design [19–21] have benefited from using probabilistic techniques. In particular, the behavior of FSMs has been investigated using concepts from the Markov chain (MC) theory where steady-state and transition probabilities are estimated for large FSMs [19,22]. This also can be achieved by repeated application of the Chapman–Kolmogorov equations [23,24].

In our approach, we used a statistical approach by simulating the state machine using random input vectors and determining the state probabilities based on it. It is done by simulating the FSMs for a sequence of 250,000 random vectors and recording the counters for each state. The resulting steady state probability is calculated by dividing those counters by 250,000 for each state.

Table 1 shows several MCNC/LGSynth FSM benchmarks [25] along with the number of states that need to be protected for achieving coverage of 50% and 90%, respectively. The results shown in the table demonstrate that for most circuits few states need to be protected to enhance their fault tolerance. For most circuits, less than 25% of the states have nearly 90% overall probability of occurrence.

The FSMs for lion9, pma and train11 are incompletely specified. To ensure correct analysis by our simulation environment, we have modified them to become completely specified by making those unspecified transitions go to the first state in the machine.

2.3. State redundancy based fault tolerance

In order to describe the proposed state redundancy based fault tolerance technique, we use an illustrative example. Then, the criteria for determining the minimum number of bits needed to encode the fault tolerant FSM is established. After that, the proposed fault tolerance minimum state encoding algorithm is presented.

2.3.1. An illustrative example

Sequential circuit reliability can be increased by adding redundant equivalent states to the FSM. The redundant states have the same input, next state, and output as the protected states. In order to illustrate this, let us consider the simple bit flipper example shown in Fig. 2. Given a FSM with two states A and B, let us assume that both states need to be protected. Originally the FSM needs only one D-FF to be implemented. To tackle single errors we add redundant equivalent states to A (A_rd0, A_rd1 and A_rd2) and to B (B_rd0, B_rd1 and B_rd2) with the same input, output and next state. For each row in the original state table, additional redundant rows are added in the protected state table as shown in Table 2.

In order to detect all single errors, the hamming distance between state A, and its redundant states should be 1. Similarly for