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A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications



Peeyush Kala*, Sudha Arora

Department of Electrical Engineering, G.B. Pant University of Agriculture & Technology, Pantnagar 263145, India

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ABSTRACT

Over the last few decades, multilevel inverters (MLIs) are being extensively utilized in many industrial and grid connected applications due to their numerous merits. With the recent development of renewable energy systems (RES), applications of classical MLI topologies are hindered due to their performance issues such as poor power quality, uneconomical structure and low efficiency. These performance issues and limitations in classical MLI topologies have attracted the researchers toward evolving new hybrid MLI topologies. In this article, a comprehensive analysis of these recent hybrid MLI topologies is done on the basis of some qualitative and quantitative performance indices. Special focus has been given to extensively review the influence of MLIs in grid connected renewable energy applications such as photovoltaic (PV) systems, wind energy conversion systems (WECS) and micro-grid. In order to provide the better insight about the working and performance of these MLI topologies, simulation results performed in MATLAB/Simulink environment are also presented.

1. Introduction

Over the years, MLIs have found their wide influence in many industrial applications such as medium voltage (MV) high power drives [1,2], active power filters [3], electric vehicles (EV) [4,5], dynamic voltage restorer (DVR) [6], unified power flow controller (UPFC) [7], micro-grid [8], power line conditioner [9], distribution static compensator (DSTATCOM) [10], stand-alone or grid integrated photo-voltaic (PV) systems [11-14], and numerous other fields. The applications of two-level voltage source inverters (VSIs) were mostly confined to lowvoltage (LV) and medium-power applications due to the voltage and power rating constraints on power semiconductor devices. Also, these pulse width modulation (PWM) inverters suffered from the high switching losses due to high frequency switching operation. These limitations gave rise to the concept of multilevel inverter (MLI) which refers to the generation of more than two voltage levels at the output of the inverter by using an array of power semiconductor devices, capacitors, and the dc voltage sources [15].

The origin of MLI concept was first coined in 1975 by Baker and Bannister. They invented a topology made of series connection of fullbridge power cells with each cell having an isolated dc source and four switches [16]. This topology was named cascaded inverter which provided a staircase AC voltage waveform at output. In 1980, Baker patented a new three-level VSI topology named as diode clamped or neutral point clamped (NPC) inverter in which diodes were used to clamp the switch voltage to the mid-point dc link voltage or voltage across a dc link capacitor [17]. Nabae et al. in 1981, implemented a new NPC inverter by utilizing pulse width modulation (PWM) technique for switching of devices [18]. In 1992, Meynard and Foch proposed a new variant of MLI named as capacitor clamped or flying capacitor (FC) MLI. This topology offered the slight modification to the NPC MLI as clamping diodes were replaced by the clamping capacitors [19]. Cascaded H-Bridge (CHB) MLI, NPC MLI, and FC MLI are called classical MLI topologies and previously well reviewed in the literature [15,20]. Each of these topologies has its own advantages and limitations. The key limitations of NPC MLI are the absence of modularity, large number of clamping diodes, unbalanced voltages, unequal switch utilization, and uneven power loss distribution with the rise in number of voltage levels [21,22]. In FC MLI, the requirement of large number of clamping capacitors and charge unbalancing of capacitors at low switching frequency are the main issues [15,23]. CHB MLI topology also has a limitation due to its requirement of large number of isolated dc voltage sources, usually batteries, PV cells, or rectifiers for generation of higher number of voltage levels [24,25]. These limitations of classical topologies paved the way for the development of novel and hybrid MLI topologies for various applications. Some of the important contributions in the MLIs are mentioned in the following sub-section.

In 2001, Peng proposed a generalized MLI topology having self-voltage balancing capability [26]. Despite its several advantages over classical topologies, this generalized topology greatly suffered due to its

E-mail address: peeyush.kala@gmail.com (P. Kala).

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^{*} Corresponding author.

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Nomenclature		V _{block, i}	total blocking voltage across ith unit	
		N _{variety}	number of variety of switches	
N _{switch}	number of switches	N_{dc}	number of dc-link capacitors	
N _{level}	number of voltage levels	V_{block}	total blocking voltage of MLI	
N _{source}	number of dc sources	n	number of cells or units	
N _{cc}	number of clamping capacitors	S, T	Switch notation	
N _{cd}	number of clamping diodes	V	DC link voltage or voltage of a dc source	
N _{diode}	number of diodes	V_D	on state voltage drop across the diode	
V_{T}	on state voltage drop across transistor	R _D	equivalent on state resistance of diode	
R _T	equivalent on state resistance of transistor	V _{load}	load voltage	
N _{comp}	number of components	N _{Cap}	total number of capacitors	
β.	constant related to transistor specification	Vc	voltage across capacitor	
G	cost factor	$V_{block,H}$	blocking voltage of H-bridge unit	
V_S	voltage across the switch		$N_{source, sub}$ number of sources in a unit or block	

uneconomical structure. For reducing the components count in CHB MLIs, selection of unequal dc voltage sources in a binary or trinary sequence manner was presented in [27-29]. Such form of cascaded topology was further classified as an asymmetric topology [30]. Barbosa et al. in 2005, proposed an active neutral point clamped (ANPC) converter topology by combining the attributes of NPC and FC MLIs [31]. Manjrekar et al. presented a novel seven-level asymmetric hybrid MLI for high power applications by cascading high voltage (HV) and slow switching integrated gate commutated thyristors (IGCTs) based H-bridge with the fast switching and low voltage insulated gate bipolar transistor (IGBT) based H-bridge inverter in 2000 [32]. Dixon et al. implemented a 27-level asymmetrical inverter based on a high frequency transformer using only single dc supply for traction drives and EVs of power rating up to 150 kW with regenerative braking capability [33]. Batschauer et al. proposed a novel three-phase hybrid MLI for MV applications in 2012 [34]. This topology employed a conventional three-phase VSI in series with half-bridge inverter at each phase which reduced the requirement of dc sources significantly. Wu and Chou in 2014, proposed a novel solar power generation system which was composed of a seven-level inverter and a boost converter [35]. In [36], authors introduced a novel symmetric hybrid MLI topology based on a three-level switching cell with reduced dc sources for medium voltage and high power applications. For PV generation systems, Rao et al. in 2015 proposed a fault tolerant single-phase fivelevel inverter consisting of a half-bridge inverter unit and three-level diode clamped inverter. This topology offered several advantages like energy balancing capability, reduction in switch count, and fault tolerant capability [37]. Recent trends in MLIs are focused on reducing the switch count, dc supplies, and gate driver circuits with the improvement in power quality and fault tolerant capability to make them economical for grid connected renewable energy applications [38].

This article critically reviews more than a hundred research papers on various MLI topologies and analyzes their ever-growing impact on grid connected renewable energy applications. The key objectives of this article are as follows:

- To comprehend about the working principles of various classical and hybrid MLI topologies.
- Performance evaluation of these MLI topologies through computer simulations and comparison tables.
- Discussion and detailed analysis of various MLI topologies in grid integrated renewable energy systems.

The structure of this article is organized as follows: Section 2, describes the terminologies and performance indices commonly used in MLIs. Section 3 provides an elaborate discussion on the working principle of classical topologies along with their comparison and simulation results, while Sections 4 and 5 discuss the classification of

recent hybrid MLI topologies along with their working principles, simulations and comparative analysis results. In Section 6, some miscellaneous MLI topologies are also discussed with their advantages and disadvantages. Section 7 provides the elaborated review on grid interfaced renewable energy applications of MLIs. Finally, Section 8 concludes the paper with remarks on future research areas related to MLIs.

2. Performance indices and terms used in MLI

In the MLI topologies, some terminologies are frequently used as described in this section.

2.1. Reduced component count topologies

MLI topologies, which have been proposed or presented with the objective of reducing the number of switches, gate driver circuits, power diodes, capacitors and other components while improving the power quality are called reduced component count topologies [38].

2.2. Modularity

Modularity means use of similar magnitude of voltage sources, similar rating of semiconductor devices and capacitors in each basic cell of MLI [28]. These similar basic unit cells are often connected in series for generation of high voltage level output. For instance, symmetric CHB MLI topology has a modular structure.

2.3. Structure of topologies

MLI topology may be symmetric or asymmetric in structure. Symmetric topology utilizes modularity whereas asymmetric topologies are aimed at reducing the size and cost of the inverter with low harmonic distortion at output voltage waveform but at the cost of loss of modularity [39].

2.4. Control complexity

This term refers to the difficulty level experienced in hardware implementation of control scheme in MLIs [40]. Asymmetric topologies generally have high degree of complexity in control.

2.5. Switch

This term means a single IGBT or MOSFET with an anti-parallel diode. It has bidirectional current carrying and unidirectional voltage blocking capability [46].

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