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Significantly improving sub-90 nm CMOSFET performances with notch-gate enhanced high tensile-stress contact etch stop layer

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ABSTRACT

This paper reports to improve performances of sub-90 nm CMOSFETs with a notch-gate structure enhanced high tensile-stress contact etch stop layer (CESL). Compared to the conventional vertical-gate CMOSFET with an additional offset spacer, the developed structure has the notch-gate as self-aligned offset spacer and lower parasitic capacitance. Beside, the notch-gate shrinks the distance of the CESL to the channel, thus enhances the channel carrier mobility more efficiently. Consequently, an n-MOSFET with this notch-gate structure showed an extra 7% I_{ON} enhancement. For p-MOSFETs, even a tensile-stress is not preferable, however, with the structure, an extra 3% I_{ON} enhancement was still achieved due to the better channel profile by halo implantation through notch-gate structure.

1. Introduction

Strain engineering has been extensively implemented for device performance enhancement since 90 nm generation and beyond. The most popular process is high tensile-stress CESL (contact etch stop layer). It improves n-MOSFETs on-current (I_{ON}) significantly [1–10], and is fully compatible with conventional CMOS process. In addition, notch-gate is a good method to reduce the overlap capacitance between gate to source/drain (S/D). It is also improves the device performance by optimizing the channel profile with halo implantation through this notch-gate structure to improve the device's short channel effects (SCE) [11]. Moreover, the influence of the CESL stress on the channel is higher through the notch-gate. Therefore, integrating the high tensile-stress CESL with a notch-gate is an efficient and simple method to obtain higher channel mobility, better SCE, and smaller parasitic capacitance simultaneously.

2. Experiments

A leading-edge 90 nm technology was used as a vehicle to demonstrate performances. For a conventional device with vertical-gate, an additional 10 nm offset spacer module was implemented. Compared with the control device, the notch-gate was produced by adding lateral poly etching on poly bottom, with 10 nm lateral notch on both sides to form a self-aligned offset spacer. After salicidation, a high tensile-stress CESL was implemented to induce higher channel stress, followed by standard contact and metallization for testing.

3. Results and discussion

The schematic view and cross section SEM for the notch-gate devices with tensile-stress CESL are shown in Figs. 1 and 2, respectively. As shown in Fig. 1, the schematic view for the notch-gate device, samples of n-metal oxide semiconductor field effect transistor (n-MOSFET) was prepared with leading-edge 90 nm CMOS technology using shallow trench isolation (STI) and a retrograde well. Following, a nitride gate oxide with an electrical oxide thickness of 16 Å was grown by rapid thermal oxidation in nitrogen oxide (NO) ambient and followed by polycrystalline silicon (poly-Si) layer deposition. For the notch-gate, lateral poly-etching was additionally performed on a poly-gate bottom, which left a 10 nm lateral notch on each side to form a self-aligned offset spacer. Then, contact etch stop layer (CESL) was implemented after salicidation to induce higher stress for device performance. As reported previously [12], due to the Poisson's effect, in a three dimensional solid, a compressive strain in one direction produces tensile stresses in the other two directions. Thus, for a n-MOSFET, the stress from the HS CESL (high tensile-stress contact etch stop layer) will induce a tensile-stress in the direction parallel to the channel to enhance the channel electron mobility due to lighter effective mass of carriers in the strained-Si layer and reduced inter-valley scattering. Beside, the notch-gate structure offers a shorten distance between the channel and the HS CESL, thus the notch-gate device has a higher induced tensile channel stress than

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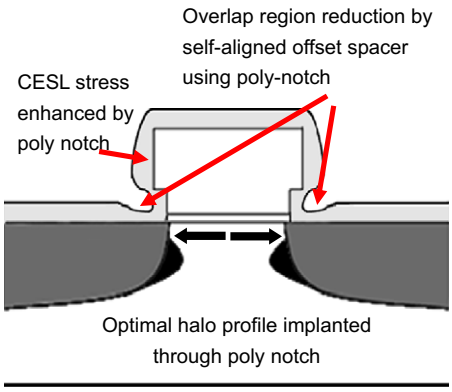

1. Poly Gate Formation
2. (a) Notch Gate Formation or
   (b) Vertical Gate + offset spacer
3. Extension S/D implantation
4. Tilted Halo Implantation
5. Source/Drain Implantation
6. Salicidation
7. Tensile Stress CESL Formation
8. Back-End Process

Fig. 1. The schematic view and process flow of the notch-gate MOSFET. Higher stress CESL induced a tensile-stress in a channel through notch-gate edge with optimal halo profile.

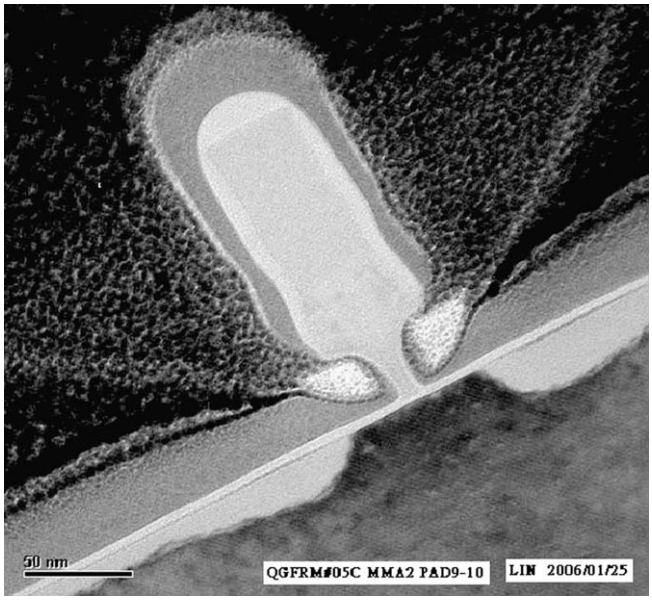

Fig. 2. Cross section SEM of the notch-gate MOSFET.

that of the conventional vertical-gate device. An extra 7% in measured driving capability of n-MOSFETs for an off current 10 nA/μm at 1 V can be obtained, as shown in Fig. 3. We believe that the increase in I_{ON} is due to the notch-gate structure enhanced CESL-induced tensile-stress. Fig. 4 shows a simulated halo profile

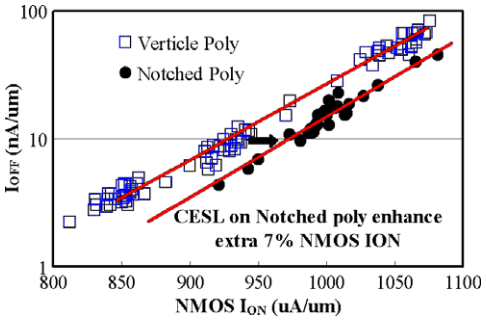

Fig. 3. The I_{ON}–I_{OFF} curves of n-MOSFET. An extra 7% improvement of I_{ON} was achieved by CESL through notch-gate.

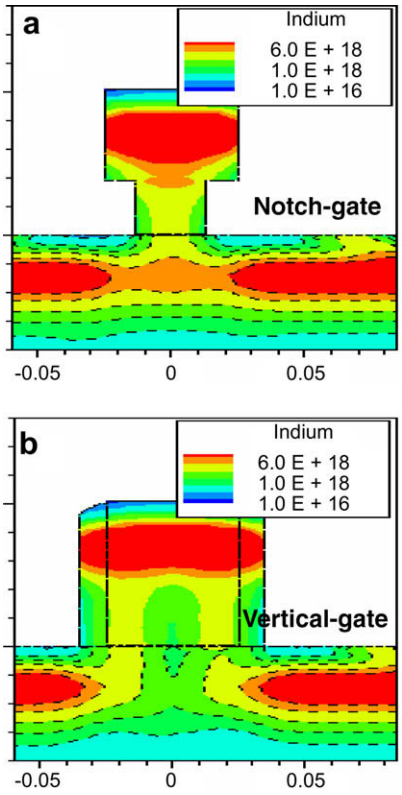

Fig. 4. Indium-halo distribution for (a) notch-gate and (b) vertical-gate n-MOSFETs. Localized halo profile can be found in the notch-gate device.

for both vertical and notch-gate 90 nm n-MOSFETs with the same threshold voltage. To improve the SCE, indium halo profile has been widely adopted in sub-micrometer n-MOSFETs for its low-diffusion constant [13–15]. It was found that a notch-gate device owns very localized indium halo profile, and thus has better Vth roll-off and DIBL (drain induced barrier lowing) characteristics, as shown in Fig. 5. Even the notch-gate device has a higher gate leakage, resulted from the higher oxide defects due to the notch-gate process and higher tensile-stress induced defect in the channel region as confirmed by the low frequency noise measurement [16–19], and shown in Fig. 6; however, the driving capability of notch-gate n-MOSFET has not been degraded significantly by these oxide defects. Compared with vertical-gate n-MOSFETs with an